January 3, 1992

To: TURBOchannel Interconnect Technology interested parties

From: Secretary, TURBOchannel Industry Group, Digital TRI/ADD Program
100 Hamilton Avenue, Palo Alto, CA 94301 U.S.A.

Re: Agenda and Proposals for 4 February 1992 meeting of TURBOchannel Industry Group

Enclosed:

- Agenda for 4 February 1992 meeting of the TURBOchannel Industry Group

  Sheraton Long Beach Hotel, 333 East Ocean Blvd.

  Long Beach, CA 90802 1.213.436.3000

- Minutes of the meeting of the December 1991 TURBOchannel Industry Group Steering Committee meeting
- Proposals for changing, modifying or clarifying the TURBOchannel interconnect specification
- Information about alternatives for the growth of TURBOchannel interconnect for discussion at the meeting

Action Requested:

1. Return attached FAX stating your commitment to attend this meeting. We must receive your response by 30 January 1992.
2. Reserve your room at the hotel under BUSCON reservations. Digital will provide complimentary exhibition badges for BUSCON. You can register for other BUSCON proceedings by contacting BUSCON at 1.800.243.3239 or 1.203.852.0500 or FAX 1.203.857.4075.
3. Read the enclosures and feel free to share this information with other people in your company. There is no restriction on the number of copies. The information is also posted for anonymous ftp on: **gatekeeper pub/TriAdd ftp address 16.1.0.2**
4. You can nominate a candidate for the TURBOchannel Industry Group Steering Committee by submitting the name of the candidate and information about him/her and his/her company on the attached form. Nominations will be accepted the day of the meeting, however it is helpful to us if you prepare this information in advance. The candidate must give **Fletcher**his/her permission to be nominated.

Information FAX for TURBOchannel Industry Group Meeting

Return to FAX 1.415.853.0155 by January 30, 1992.

Confirmation to attend TURBOchannel Industry Group Meeting 4 February 1992

Name ____

Company ____

Phone ______________________ FAX ___________________

My company will **NOT** be represented at the TURBOchannel Industry Group.

Name ____

Company ____

Remove my name from the TURBOchannel interest group.

Name ____

Company ____

Remove my company from the TURBOchannel interest list.

Name ____

Company ____

I want to **nominate** the following candidate for the TURBOchannel Industry Group Steering Committee (attach separate page with information):

Name ____

Company _______________________________________

Phone ____

I want to make a **presentation** during the Open Forum session at the 4 February 1992 TURBOchannel Industry Group meeting.

Name ____

Company ____

Phone ____

Agenda

4 February 1992

TURBOchannel Industry Group Meeting

Dr. Bill Fletcher, President, Design Analysis Associates, Chair

Dr. Dileep Bhandarkar, Digital Equipment Corporation, Co-chair

Brenda Christensen, Digital Equipment Corporation, TRI/ADD Program representative to the TURBOchannel Industry Group

8:30 am registration

9:00 am meeting starts

Opening Remarks **Bill Fletcher, Chair**

Presentation of nominations for 6-member steering committee

2 - 1 year term

2 - 2 year term

2 - 3 year term

Nominations from the floor or mail-in nominations for election of 3 members of Industry Group to serve on Steering Committee

1 - 1 year term

1 - 2 year term

1 - 3 year term

Voting 9 member steering committee

Presentation of recommendation for TURBOchannel Architecture ECO process *(as outlined in the minutes of the TURBOchannel Industry Group Steering Committee, December, 1991)*

Discussion and vote on ECO process

TURBOchannel Industry Group Meeting Agenda - 4 February 1992

Presentation of proposals for revision to TURBOchannel Architecture specification

I/O read byte masking proposal (by Digital Equipment - Bob Prevett)

Parity support proposal (by Digital Equipment - Bob Prevett)

DC Threshold voltage proposal (by Digital Equipment - Bob Prevett)

Floating bus restriction proposal (by Digital Equipment - Bob Prevett)

Discussion on proposals for revision

Voting on proposals Steering Committee

Lunch

Open Forum:

Discussion on alternatives to increase the performance and future growth of TURBOchannel interconnect. *Please note - we encourage and invite participation in these alternatives for enhancing the TURBOchannel interconnect technology. Digital Equipment is welcoming your ideas in the early stages of Digital internal discussions on the growth of TURBOchannel. If you and your company have ideas you would like to share please contact the TRI/ADD Program by 30 January 1992. Time allocations are planned for additional topics.*

(45 minutes) Block I/O Write (by Digital Equipment - John DeRosa)

(45 minutes) Speed Selectable TURBOchannel (by Digital Equipment - Bob Prevett)

(45 minutes) Extended TURBOChannel (by Digital Equipment - Chris Cuenod)

Conclusion

TURBOchannel Industry Group Steering Committee

Minutes of the meeting 5 December 1991

Topics discussed at the meeting included:

- **TURBOchannel Industry Group Process**
- **TURBOchannel Industry Group Steering Committee Functions**
- **TURBOchannel Architecture Management Process**

TURBOchannel Industry Group

The TURBOchannel Industry Group membership consists of all companies registered, at no cost, in Digital's TRI/ADD Program. All technical and business contacts registered with TURBOchannel interest in the TRI/ADD Program will receive written documents pertaining to the TURBOchannel Industry Group.

The TURBOchannel Industry Group reviews requests to enhance, clarify, or modify TURBOchannel architecture. It is the **intent** of the TURBOchannel Industry Group to

- Maintain forward compatibility of all TURBOchannel options.
- Minimize obsolescence of any TURBOchannel option.
- Maintain the TURBOchannel specification as a simple, easy to implement, stable technology in the spirit of its design.
- Contribute to the technical longevity of the TURBOchannel architecture.

Responsibilities of the TURBOchannel Industry Group

Digital Equipment Corporation will maintain the master document of the TURBOchannel specifications.

No changes to the TURBOchannel architecture specification will be made without review by the industry clearing house - called the TURBOchannel Industry Group. Changes and modifications to the specification will be based on how the changes might affect existing options and compatibility.

The TURBOchannel Industry Group will include a Steering Committee which makes the Group's final recommendations to Digital Equipment Corporation about changes to the TURBOchannel architecture master document.

TURBOchannel Industry Group Meetings

An annual meeting of the TURBOchannel Industry Group will be held at a time and place to be announced no later than 90 days before meeting is commenced. Additional TURBOchannel Industry Group meetings may be called with a minimum 30 days notice by the TURBOchannel Industry Group Steering Committee.

TURBOchannel Industry Group Steering Committee

There will be a Steering Committee of the TURBOchannel Industry Group consisting of 9 members: Six (6) members must have TURBOchannel options or systems shipping. Three (3) members will be elected from the TURBOchannel Industry Group. The Chair of the Steering Committee will be elected from among the committee by the members.

Members of the Steering Committee will serve a 3-year term, with 3 new members joining the committee annually. 2 of the 6 steering team members with shipping TURBOchannel options or systems will rotate annually. 1 of the 3 members elected from the TURBOchannel Industry Group will rotate annually.

A member of Digital's TRI/ADD Program will serve as Secretary to the Steering Committee.

Members must attend or send a representative to at least 1 meeting a year of the Steering Committee. If this minimum attendance is not maintained they will have been deemed resigned.

Meetings of the TURBOchannel Industry Group Steering Committee

In addition to meeting at the time and place of the annual TURBOchannel Industry Group meeting, the Chair may call additional meetings of the TURBOchannel Industry Group Steering Committee. Individual persons in the steering committee may also request the chair to hold a meeting by notifying the chair of this request in writing. The meeting can be held with a minimum 30-day notice and no later than 90 days from the requester's notification. The Secretary of the Steering Committee maintains minutes of all Steering Committee meetings, which will be published for all members of the TURBOchannel Industry Group.

A company may have no more than one representative on the TURBOchannel Industry Group Steering Committee.

TURBOchannel Industry Group Support

Digital's TRI/ADD Program will provide executive and administrative support to the TURBOchannel Industry Group and TURBOchannel Industry Group Steering Committee. This support includes receipt and dissemination of all materials and documents to the TURBOchannel Industry Group and the TURBOchannel Industry Group Steering Committee members. The TRI/ADD Program will maintain documentation related to receipt of all proposals and there will be a system maintained to track the proposals.

Written Documentation

All information will be supplied in written form either through electronic access or printed copy. FAX information will also be acceptable although the original copy must be sent to the Secretary following receipt of Fax.

TURBOchannel Industry Group Process

TURBOchannel Architecture Engineering Change Order (ECO) Process

An originator of a request to modify or clarify the TURBOchannel architecture specification must do so in writing. Incomplete proposals will be returned. The following information must be included in the proposal:

- Description of functional changes and the benefits of those changes
- Impact to existing options and systems that conform to the specification
- Hardware implications. Software implications.

See Diagram A for general steps in the ECO process.

The written request is sent to the Secretary of the TURBOchannel Industry Group Steering Committee.

c/o Secretary, TURBOchannel Industry Group Steering Committee
TRI/ADD Program
Digital Equipment Corporation
100 Hamilton Avenue
Palo Alto, CA 94301 U.S.A.

The Secretary organizes written requests and sends written documentation of the proposal(s) to the TURBOchannel Industry Group membership. The membership has 30 days to review the request for change and send it back to the Secretary. One of four responses is acceptable:

1. Agreement
2. Agreement, with changes in writing
3. Disagreement, for the following reasons
4. Abstention

The Secretary compiles the members' responses and sends all their inputs back to the Originator of the request and to the Steering Committee. The Steering

Committee members then review all recommendations and vote for:

1. Approval
2. Approval, with Changes
3. Disapproval for the following reasons
4. Abstention
5. Call for a meeting to discuss

The Secretary compiles the results of the vote. The Chair notifies all TURBOchannel Industry Group members of the voting results by way of the Secretary. Each Industry Group member has 30 days to protest or appeal the vote. A protest or appeal must be made in writing to the Secretary. After the 30 days, if there is no protest or appeal, the Chair submits the change to Digital Equipment Corporation for incorporation into the master document.

Redraft of Original Request

The originator of a request that was disapproved can redraft the original request and starts the process again.

Appeal Process

The originator of a request that is disapproved can appeal to the TURBOchannel Industry Group Steering Committee. The appeal must be made in writing to the Secretary.

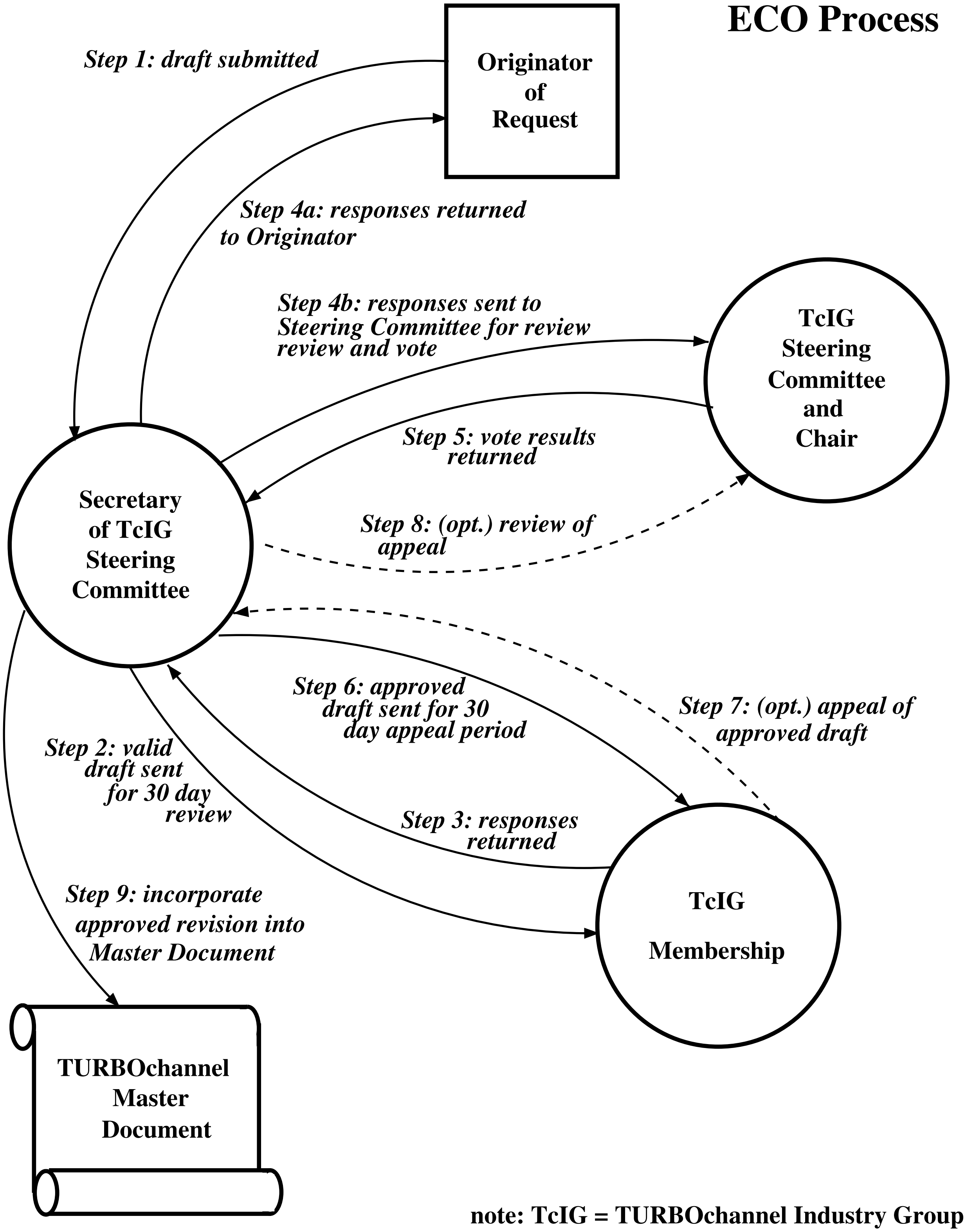
Proposals without Merit

If the Secretary deems a request to be inappropriate, the Secretary sends the proposal to the Chair of the TURBOchannel Industry Group Steering Committee. The Chair then determines whether the request for change is frivolous. The originator will be sent notice that the document will not be forwarded for review. The Originator can appeal to the Chair. If the Chair determines the request for change is not frivolous, it will go through the regular dissemination process for Industry Group review.

Conformance Certification

The TURBOchannel Industry Group, the TURBOchannel Industry Group Steering Committee and/or Digital Equipment's TRI/ADD Program will **NOT** provide certification programs for compliance testing.

TURBOchannel Architecture ECO Process



note: TcIG = TURBOchannel Industry Group

Diagram C

100 Hamilton Avenue
Palo Alto, CA 94301
December 14, 1991

TURBOchannel Industry Group
Steering Committee
c/o TRI/ADD Program
Digital Equipment Corporation
100 Hamilton Avenue
Palo Alto, CA 94301

To the Secretary:

Please distribute this Proposal to the TURBOchannel Industry Group membership for the thirty day review period.

Sincerely,

Robert J. Prevett, Jr.
Digital Equipment Corporation

Proposal for Change to the TURBOchannel Specification: Parity

- Description of functional changes and the benefits of those changes:

Use of parity on TURBOchannel will help to verify data integrity for the transfer of data between options and systems. Parity is an optional feature that is implemented when determined as necessary by the system or option designer. This Proposal specifies the details of TURBOchannel parity implementations.

1) Systems and options that support parity must always supply valid parity when they drive the ad bus. All 32 ad lines are used for parity generation and checking. Odd-word parity is used: the number of one's in ad[P,31..0] must be an odd number.

2) When ~reset is asserted, systems and options must disable parity checking of the ad bus.

3) When a system that supports parity configures a TURBOchannel slot at system startup, it should examine each option ROM flags field. If bit flags<0> has the value one, then the system should enable parity checking for that option slot.

4) When an option that supports parity executes the firmware init routine, the option should execute the gettcinfo callback; if the parity field is non-zero, then the option should enable parity checking.

The following sections discuss parity error response for the various transaction types, assuming that both system and option have ad bus parity checking enabled.

I/O Reads:

There is no mechanism for an option to return an explicit error acknowledgement if it detects a parity error in the slot address/mask. Hence, the option should generate a parity error interrupt and let the I/O read transaction timeout. The option TURBOchannel interface should not issue the read to its internal logic.

If the system detects a parity error in the I/O read data, it should generate a parity error interrupt and signal a bus error to the processor.

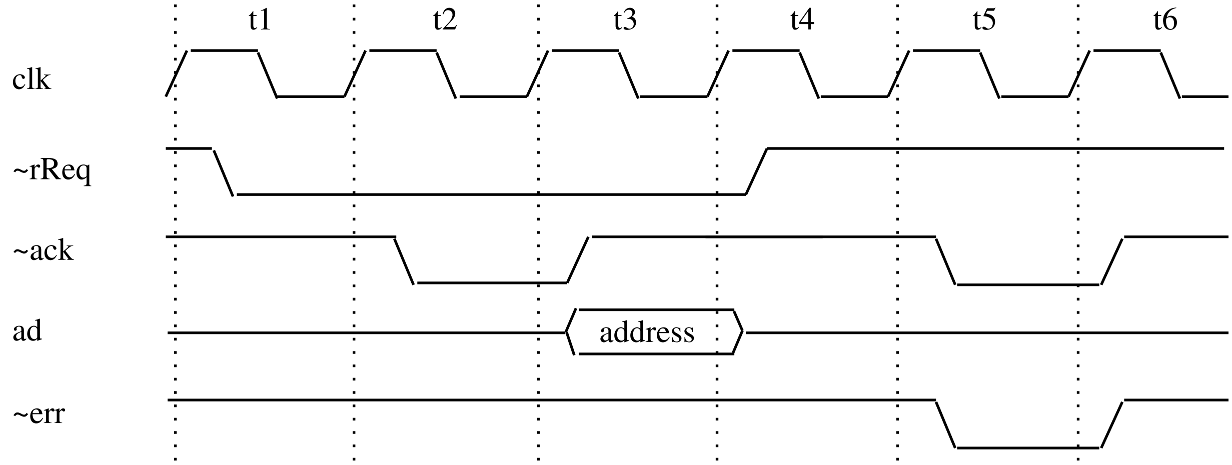
I/O Writes:

There is no mechanism for an option to return an explicit error acknowledgement if it detects a parity error in the slot address/mask or data. Hence, the option should generate a parity error interrupt. It is also recommended that the option TURBOchannel interface ignore the write data and not issue the write to its internal logic.

DMA Reads:

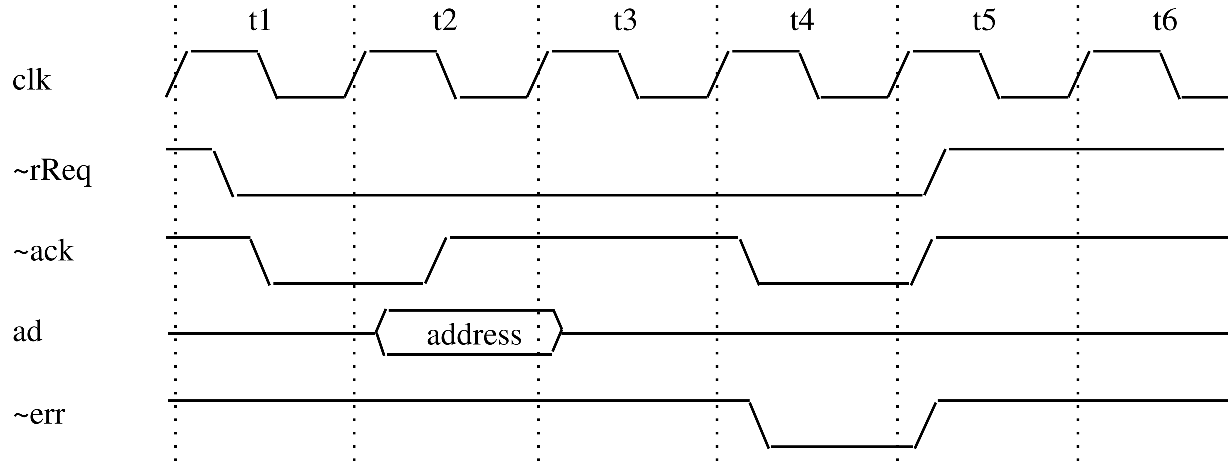
There is no mechanism for the system to explicitly signal a parity error of the DMA address. Hence, the system should assert ~ack and ~err for a period of one cycle following the address transfer. The system TURBOchannel interface should generate a parity error interrupt. It is recommended that the system TURBOchannel interface not issue the read to the memory system. The option must terminate its DMA transaction on the cycle immediately after the ~err signal is asserted. The option TURBOchannel interface should generate a DMA error interrupt. The option TURBOchannel interface should indicate an error to its internal logic.

DMA read of 1 word with address parity error:



t1: option requests a dma cycle
t2: option is granted the bus
t3: option drives address onto ad
t4: system memory latency (may be many cycles)
t5: system has detected ad parity error and asserts ~ack and ~err
t6: idle cycle

DMA read of 4 words with address parity error (aborted after 3 words have been requested):



t1: option requests and is granted dma access
t2: option drives address onto ad
t3: system memory latency
t4: system has detected ad parity error and asserts ~ack and ~err
t5: option deasserts ~rReq in response to ~err
t6: idle cycle

If an uncorrectable memory error occurs during the DMA read transaction, the system asserts ~err along with the uncorrectable data.

If an option TURBOchannel interface detects a data parity error, it should generate a parity error interrupt, abort the transaction, and indicate an error to its internal logic.

DMA Writes:

There is no mechanism for the system to explicitly signal a parity error of the DMA address or data. Hence, the system TURBOchannel interface should generate a parity error interrupt. The system TURBOchannel interface should not write the affected word(s) to the memory system.

Error Logging:

It is recommended that parity options and systems log the transaction type (I/O versus DMA), the transaction direction (read versus write), the transaction phase (address versus data), and the ad bus value when they detect a parity error.

- Impact to existing options and systems that conform to the Specification:

Existing options and systems do not support parity; the impact to these options and systems is minimal. Options and systems currently under development that implement parity may not be fully compliant with this proposal.

- Hardware and software implications:

Implementation of parity will require additional complexity in both the system and option interfaces; parity generation and checking circuitry must be added. System software will be required to handle parity errors at the system TURBOchannel interface; option device driver software will be required to handle parity errors at the option TURBOchannel interface.

100 Hamilton Avenue
Palo Alto, CA 94301
December 12, 1991

TURBOchannel Industry Group
Steering Committee
c/o TRI/ADD Program
Digital Equipment Corporation
100 Hamilton Avenue
Palo Alto, CA 94301

To the Secretary:

Please distribute this Proposal to the TURBOchannel Industry Group membership for the thirty day review period.

Sincerely,

Robert J. Prevett, Jr.
Digital Equipment Corporation

Proposal for Change to the TURBOchannel Specification: I/O Read Byte Masking

- Description of functional changes and the benefits of those changes:

The TURBOchannel Hardware Specification needs to be enhanced to include byte masking for I/O read transactions. This feature is necessary for options that require knowledge of the requested data word size. Such options include TURBOchannel adapters to buses with variable word sizes, like VME.

The second and third paragraphs of the I/O Addressing section in the TURBOchannel Hardware Specification will be modified and consolidated to read:

"Figure 1-3 shows the interpretation of the ad signals during an I/O transaction. Bits ad [31..5] specify the word address within the slot space. Bits ad[4..1] specify the byte masks for the ad signals during the subsequent data cycle of the transaction. If a byte mask bit is one for an I/O write transaction, the corresponding byte lane is not stored in the addressed option word. If a byte mask bit is one for an I/O read transaction, the corresponding masked byte lane may contain invalid data. The option is only required to return valid data for unmasked byte lanes. However, the option must still drive the masked ad lines to logic one or zero; the ad lines corresponding to masked byte lanes must not be left tristated during the data cycle."

The current Figure 1-3 - Interpretation of the ad signal during an I/O read - will be deleted from the TURBOchannel Hardware Specification. The current Figure 1-4 will become the new Figure 1-3 and will be updated to read "Figure 1-3. Interpretation of the ad signal during an I/O transaction."

- Impact to existing options and systems that conform to the Specification:

There is no impact to existing options. Options that do not utilize I/O read byte masks - the vast majority of options - will return the full requested data word. This is in compliance with the proposal.

There will be an impact to existing systems. Existing systems that do not implement I/O read byte masks will not function with options that utilize I/O read byte masks. The system vendor will identify in the System Parameters section of the TURBOchannel Specification whether or not I/O read byte masking is implemented. All new TURBOchannel systems will be designed to incorporate I/O read byte masks.

- Hardware and software implications:

Implementation of I/O read byte masking will require a slightly increased level of hardware complexity for both system and option interfaces. The software implications are dependent upon the platform implementation. For a processor with byte and double-byte operations, I/O read byte masking could be made relatively transparent to software. There will be a larger software impact for processors without such operations.

100 Hamilton Avenue
Palo Alto, CA 94301
December 13, 1991

TURBOchannel Industry Group
Steering Committee
c/o TRI/ADD Program
Digital Equipment Corporation
100 Hamilton Avenue
Palo Alto, CA 94301

To the Secretary:

Please distribute this Proposal to the TURBOchannel Industry Group membership for the thirty day review period.

Sincerely,

Robert J. Prevett, Jr.
Digital Equipment Corporation

Proposal for Change to the TURBOchannel Specification: DC Threshold Voltage

- Description of functional changes and the benefits of those changes:

The TURBOchannel Hardware Specification does not currently specify how the timing requirements of signals are to be measured. Specification of a DC threshold voltage will allow for more consistent and accurate measurement of TURBOchannel timing parameters. A voltage threshold for input and output signals will be specified:

$$\mathbf{Vti = Vto = 1.4V}$$

The timing of a TURBOchannel signal will be measured with respect to the threshold values. For instance, the 7ns max. time for clk to ~rReq will be measured from the clk signal reaching Vti (1.4V) to the ~rReq signal reaching Vto (1.4V).

- Impact to existing options and systems that conform to the Specification:

Existing options and systems that conform to the Specification will not be impacted. There is a slight risk that the method of measurement used for existing options and systems demonstrated conformance to Hardware Specification while those devices may now not conform with this standard method of measurement.

- Hardware and software implications:

This method of AC performance measurement is fairly standard and allows for straightforward timing parameter measurement. There are no software implications

100 Hamilton Avenue
Palo Alto, CA 94301
December 12, 1991

TURBOchannel Industry Group
Steering Committee
c/o TRI/ADD Program
Digital Equipment Corporation
100 Hamilton Avenue
Palo Alto, CA 94301

To the Secretary:

Please distribute this Proposal to the TURBOchannel Industry Group membership for the thirty day review period.

Sincerely,

Robert J. Prevett, Jr.
Digital Equipment Corporation

Proposal for Clarification to the TURBOchannel Specification: Floating Bus Clarification

- Description of functional changes and the benefits of those changes:

The TURBOchannel ad bus must not be left floating for more that one TURBOchannel clock period. This requirement is implied by timing diagrams in the Hardware Specification but should be explained more clearly. To better clarify this requirement, the following text will be added to the Implementation Notes section of the TURBOchannel Hardware Specification:

"The ad bus should not be left floating for more than one TURBOchannel clock period. When the TURBOchannel is idle, the system must drive the ad[P,31..0] lines. After an I/O read address has been sent and the bus has been turned around, the option must drive the ad lines until the valid data is ready. Referring to the I/O read timing diagram, Figure 1-1, the option must drive the ad bus during the t3 cycle(s). The ad bus will float during the t2 cycle to avoid bus contention. After a DMA read address has been sent by the option and the bus has been turned around, the system must drive the ad lines until the DMA read data is ready. Referring to the One-word DMA read timing diagram, Figure 1-6, the system will drive the ad bus if additional t3 cycles are required due to memory access latency. The ad bus will float during the first t3 cycle to avoid bus contention.

"TURBOchannel options and systems must drive the parity line to a valid logic state when driving the ad lines so that the parity line will not float. For systems and options that do not implement parity, the logic value of this parity line need not be the correct parity value."

Figure 1-1 of the TURBOchannel Hardware Specification, I/O read of an option by the system, will be clarified to indicate that the data of cycle t3 is only required to be a valid logic state and not required to be the valid read data word.

- Impact to existing options and systems that conform to the Specification:

There is no impact to systems and options that currently drive the parity line to a valid logic state. Existing systems and options that do not drive the parity line will be in violation of this proposal. If options that drive the parity line are installed in systems that do not drive the parity, the parity line receiver of the option will float under certain conditions. Similarly, if options that do not drive the parity line are installed in systems that do drive the parity line, the parity line receiver of the system will float under certain conditions.

- Hardware and software implications:

Systems or options that allow the ad lines to float for more than one TURBOchannel clock period pose device reliability and power dissipation risks to the receivers of CMOS bidirectional transceivers. Therefore, the Hardware Specification should be made more clear on this issue to eliminate non-compliance. A second hardware implication is that the options and systems now require some additional circuitry to drive the parity line.

There are no software implications.

For Discussion Only - Not Submitted for Voting

100 Hamilton Avenue
Palo Alto, CA 94301
January 2, 1992

TURBOchannel Industry Group
Steering Committee
c/o TRI/ADD Program
Digital Equipment Corporation
100 Hamilton Avenue
Palo Alto, CA 94301

To the Secretary:

Please distribute this Proposal for Speed Selectable TURBOchannel to the TURBOchannel Industry Group membership in preparation for the discussion of this topic at BUSCON in the first week of February 1992.

Sincerely,

Robert J. Prevett, Jr.
Digital Equipment Corporation

Proposal for Enhancement to the TURBOchannel Specification: Speed Selectable TURBOchannel

The TURBOchannel uses a free-running clock, tc.clk, at any fixed frequency from 12.5 to 25 MHz. A speed selectable TURBOchannel would be able to run up to 50 MHz using the same signaling protocol. The system would power up at 25MHz and then read the flags field of the option ROM to see if the option were capable of supporting a higher rate of tc.clk. If the option was capable of doing so, the system would selectively turn up the clock rate to that option; the option would then be reset. This requires that the configurable TURBOchannel option slots in any system have a radial implementation (that there be a separate TURBOchannel to each option slot).

For Discussion Only - Not Submitted for Voting

146 Main Street
Maynard, MA 01754
January 2, 1992

TURBOchannel Industry Group
Steering Committee
c/o TRI/ADD Program
Digital Equipment Corporation
100 Hamilton Avenue
Palo Alto, CA 94301

To the Secretary:

Please distribute this Proposal for TURBOchannel Block I/O Writes to the TURBOchannel Industry Group membership in preparation for the discussion of this topic at BUSCON in early February 1992.

Sincerely,

John A. DeRosa
Consultant Engineer
Digital Equipment Corporation

Proposal for Modification to the TURBOchannel Specification: Block I/O Write

- Description of functional changes and the benefits of those changes:

This is a proposal for a change to the TURBOchannel architecture to allow the addition of Block I/O Writes. The modifications required of the TURBOchannel Specification to incorporate this change are as follows:

I) Add the following paragraphs to the "I/O Transactions" section, which starts on page 1-2:

<u>Block I/O Writes</u>

A variant of I/O write, called "Block I/O write", is an optional part of the architecture. A system's documentation package must specify:

* whether they are implemented by the system.

* the maximum block size supported, up to the architected limit of 64 words.

For Discussion Only - Not Submitted for Voting

If implemented, software must be able to enable them on a per-slot basis. A system must provide a way for software to limit a Block I/O write's size to that handled by an option.

A TURBOchannel option that supports Block I/O writes must document this in its documentation. (No option ROM fields are needed, since a driver for a device will be written with the a priori knowledge of that device's support of Block I/O writes.) An option must be able to work correctly in systems that do not implement Block I/O writes, and it must be able to work correctly with any combination of normal and Block writes. An option's documentation must specify the maximum size Block supported.

Block I/O writes may be used by an option's ROM diagnostics. This means that the system must be able to provide information back to the option on its Block I/O write capabilities through the gettcinfo system callback routine; the definition of the new gettcinfo field is TBD. Also, the system must provide a generic way for option ROM code to generate Block I/O writes. This could be done with system module callbacks similar to testintr. The definition of this new system module callback is TBD.

The data words in a Block I/O write must be written by the option in the order received.

The section on Block I/O writes describes in detail the signaling of the transaction."

II) Insert the following section between the I/O write and I/O addressing descriptions, on page 1-8:

Block I/O Write to an Option by the System

Block I/O Writes make use of a different behavior in the ~sel and ~write signals to indicate that a block of I/O write data is being sent to the option, instead of a single longword. Think of this as DMA initiated from the system instead of the I/O device.

The benefits in bandwidth may be computed as follows.

Let W = the number of words to be written over the TURBOchannel.

Let R = 0 if the option can assert ~rdy in cycle t2 of an I/O write
1 if the option can assert ~rdy in cycle t3 of an I/O write
2 if the option can assert ~rdy in cycle t4 of an I/O write
(etc.)

The number of TURBOchannel cycles required to write W words using regular I/O writes is:

reg_cycles = W (3 + R)

The number of TURBOchannel cycles required to write W words using Block I/O writes is:

block_cycles = W + R + 3

The bandwidths for R=0 options on a 25 MHz TURBOchannel are:

Number of Words Being Written	Normal I/O Cycles	Writes Bandwidth MB/sec	Block I/O Cycles	Write Bandwidth MB/sec
2	6	33	5	40
4	12	33	7	57
8	24	33	11	73
16	48	33	19	84
32	96	33	35	91

It is true that the CPU is dedicated to pushing out these I/O writes. But it must also issue writes to memory to prepare for an option's DMA read. Hence, a block I/O write will be preferable over a DMA-based approach for some applications, both for memory & I/O bandwidth considerations and the option hardware complexity.

We will now describe how a Block I/O write behaves.

The beginning of a Block I/O write looks just like a normal I/O write. Figure xxx-xxx shows an example of a 6-word Block I/O write.

1. Cycle t1

This is the same as cycle t1 of Figure 1-2.

2. Cycle t2

This is the same as cycle t2 of Figure 1-2. The data word being sent is word #1.

There are zero (0) or more t2 cycles.

3. Cycle t3.

The options asserts ~rdy here.

If the option cannot accept a normal I/O write, it would also assert ~conflict here.

If the option supports Block I/O writes and it is not sure that it could accept the maximum possible block size, it MUST assert ~conflict here. Block I/O Writes allow ~conflict to be asserted only during the first ~rdy cycle.

4. Cycle t4.

The system continues to drive the ad<31:0,p> lines with legal voltage values, but the contents of these lines are unpredictable in this cycle.

The fact that ~sel and ~write are not deasserted in this cycle is what indicates to the option that this is a Block I/O write.

(If the option had asserted ~rdy and ~conflict in cycle t3, this would be an inter-transaction idle cycle.)

5. Cycles t5 - t9.

The system sends words #2 - #6, one per cycle. No handshaking is performed.

~sel and ~write remain asserted. A Block I/O write's length is indicated by the number of cycles that ~sel and ~write are true.

6. Cycle t10.

In the cycle after word #6, the system deasserts ~sel and ~write, and may assert ~ack for a pending DMA request.

This is the same as cycle t4 of Figure 1-2."

III) Add the following text to the I/O Addressing section on page 1-8:

"The address for a Block I/O write is the address of the first word supplied in the write. Successive words are written to monotonically increasing addresses. The address has the same format as normal I/O reads and writes, which means that the byte mask is applied to every word written."

IV) Add something like the following to the new parity / ~err section:

"If a parity error is detected in any of the words in a Block I/O write, the option will interrupt (~int) the system."

- Impact to existing options and systems that conform to the Specification:

There should be no impact to existing options and systems that conform to the spec. Reasons:

a. All options that implement Block I/O writes MUST function correctly in systems that do not support Block I/O writes. It is acceptable that performance suffers when such an option card is used in a non Block I/O write system.

b. All systems supporting Block I/O writes must also support the standard, mandatory one-word I/O write.

c. System designers implementing Block I/O Writes should provide them with a minimum impact on software. Ideally, application software should not have to do anything special to use Block I/O Writes.

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- Hardware and software implications:

It is strongly suggested that systems be designed such that applications do not have to behave differently in order to take advantage of Block I/O writes.

A way to do this is to use one or more write data buffers between the CPU and the TURBOchannel. I/O writes to addresses outside the buffer(s) would cause the current buffer contents to be dumped to the TURBOchannel; otherwise, the I/O write data is held in the buffer. If the system doesn't provide any other means of purging the buffer(s), then they would be purged on an I/O read and/or during periods when the system is idle. This kind of scheme allows CPU I/O writes to be accumulated without explicit software intervention (so that they may be bursted as a Block I/O write) while naturally supporting single-word writes. The hardware cost: buffer space, address matching hardware, per-slot "block I/O write enable" bits in a system register, and additional I/O write state machine complexity. But depending on how the CPU manages its write buffers, much of this cost may already be paid for.

Software implications: The operating system must determine what option slots support Block I/O writes and set system register bits accordingly. In the system design described in the previous paragraph, application software would not need any knowledge of how the I/O writes were being serviced.

If a system supports block I/O writes by some explicit mechanism, like alternate I/O address spaces, then some software would have to behave differently to take advantage of Block I/O writes. This kind of implementation is strongly discouraged.