Integrated Diagnostic Environment (IDE) Reference Guide

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Contents

Introduction

This document contains information about the Silicon Graphics service tool IDE, the Integrated Diagnostic Environment. This information includes a general product overview; instructions on installation, configuration, and operation of this program; and descriptions of the test suite.

The following typographic conventions are used throughout this document:

Convention	Meaning
`TYPEWRITER FONT`	Denotes literal items such as command names, file names, routines, directory names, path names, signals, messages, and programming language structures.
italic font	Denotes variable entries and words or concepts being defined.
`bold typewriter font`	In screen drawings of interactive sessions, denotes literal items entered by the user. Output is shown in nonbold typewriter font.
[]	Indicates an optional item.
<>	Indicates a required variable within an optional item.

Within this document, reference is made to the online man pages that are available under the IRIX operating system through the `man` command. A *man page* is a discussion of a particular element of the IRIX operating system or a compatible product.

Each man page includes a general description of one or more commands, routines, or other topics and provides details of their usage (command syntax, routine parameters, system call arguments, and so on). If more than one topic appears on a page, the entry will appear in the printed manual alphabetized only under its major name. You can access a man page named `ls` online by typing `man ls`.

Man pages are grouped into sections that are numbered from 1 to 8. Each section contains entries of a particular type. Types of entries include user commands (1), administrator commands (8), system calls (2), library routines (3), file formats (5), and device descriptions (4).

Section numbers appear in parentheses after man page names. Man pages are referenced in text by entry name and section number.

Chapter 1

Introduction to Octane_ide

This Chapter provides an overview of the Integrated Diagnostic Environment (IDE), and lists the diagnostics that you can use to troubleshoot failures on the IP30 OCTANE system.

1.1 Product Overview

Octane_ide is a standalone diagnostic environment with which you can diagnose failing hardware components on an OCTANE system. It enables you to run diagnostic tests in an environment that cannot be accessed from a user program that is running under the IRIX operating system.

Octane_ide diagnostics require a dedicated OCTANE system; you must reboot the system to run Octane_ide. In other words, the IRIX operating system cannot be running when you use Octane_ide diagnostics. You should use Octane_ide diagnostics to diagnose failures when IRIX based diagnostics do not provide sufficient error information, or to isolate failing hardware that IRIX based diagnostics cannot test.

This document describes Octane_ide version 1.0.

1.2 Diagnostic Tests

Octane_ide diagnostics are directed tests; each test focuses on a specific area of the system. These test areas include the IP30 processor board, the system NIC (number-in-a-can), the front plane, the processor module, the graphic circuits, and the PCI shoebox.

Note: Your system must contain the appropriate hardware for the PCI shoebox test to operate properly. If you attempt to run the PCI Shoebox test without a PCI Shoebox, Octanne_ide will fail with a fatal exception and you must reboot Octane_ide to reestablish the diagnostic environment.

1.2.1 IP30 Processor Tests (ip30)

ip30 tests the following components within each IP30 processor:

- Number-In-a-Can (NIC)
- Heart
- Bridge
- XBOW
- Memory
- RAD (built-in audio)
- IOC3
- RTC
- DUART

1.2.2 Processor Module Tests (pm)

pm tests the following components:

- Number-In-a-Can (NIC)
- TLB
- TLB Exception
- Data Cache Data Parity
- Icache
- Secondary Cache ECC RAM / Interrupt
- Secondary Cache Data and Address
- FPU
- lpackd

1.2.3 Front Plane Tests (fp)

fp tests the following components:

- Front Plane
- XBOW

1.2.4 Graphics Tests (gfx)

Refer to paragraph 7.1 for a list of components that gfx tests.

1.2.5 TRAM Tests (mg_test_tram)

`mg_test_tram` is a subtest of the gfx diagnostic, which can be run independently of gfx.

1.2.6 PCI Shoebox Tests (shoebox)

shoebox tests the PCI Shoebox.

1.3 Installing and Configuring Octane_ide

Use the following procedure to install and configure Octane_ide.

1. The Internal Support Tools CD1.2 Web release includes version 1.0 of Octane_ide. Refer to the instructions included in the release package for information about how to install Octane_ide software in the `/stand` directory on your system disk.
2. After you have installed Octane_ide software on your system disk, you must set the following NVRAM variable from either the Command Monitor or from the IRIX operating system:

   `>>`**`setenv ge_ucode_from_disk 1`**

   or

   `#` **`nvram ge_ucode_from_disk 1`**

   Note: If you do not set the ge_ucode_from_disk 1 variable, the gfx test will fail.
3. Use the `boot` command to load Octane_ide
4. On the system that you wish to test, enter the following command:

   `>>`**`boot dksc(x,y,z)/stand/Octane_ide`**

   where *x*, *y*, and *z* refer to the controller, disk and slice number of the disk where Octane_ide is installed.
5. At the ide> prompt that appears, enter the following command:

   `ide>>`**`list`**

   Note: You must enter the `list` command to set environmental variables before you run any tests. The `list` command also displays the list of diagnostics.

Future updates to Octane_ide diagnostics will be available at the Internal Support Tools group Web site or on future CD releases. Refer to:

http: / / ist.csd.sgi.com / Tools / Home_pages / products_main.html

After you boot Octane_ide from the Comand Monitor (that is, at the BaseIO command prompt, >>), the `ide>>` prompt appears. At this prompt, you can enter commands that control Octane_ide and commands that run diagnostic tests.

Chapter 2

Commands that Control Octane_ide

Although there are many commands and diagnostics that are available within Octane_ide, please use only the commands that are documented in this manual. Some diagnostics have prerequisite tests, commands, and environmental variables that must be set for them to run correctly. If you run the undocumented tests without proper initialization, you may leave Octane_ide in an unknown state or cause an Octane_ide exception.

2.1 hinv Command

The `hinv` command displays the contents of the system hardware inventory table. This table is created each time the system is booted and contains entries that describe the various hardware components in the system. The items in the table include the main memory size, cache sizes, floating-point unit, and disk drives. Without arguments, the `hinv` command displays a one-line description of each entry in the table. This command uses the following syntax:

```
hinv
```

2.2 printenv Command

The `printenv` command displays all current NVRAM variable settings if you enter it without arguments or it displays the value of a single specified NVRAM variable. This command uses the following syntax:

```
printenv
```

or

```
printenv [<variable>]
```

2.3 setenv Command

The `setenv` command sets a selected variable that is stored in NVRAM to a specified value. This command uses the following syntax:

```
setenv <variable> <value>
```

2.4 unsetenv Command

The `unsetenv` command clears a selected variable that is stored in NVRAM. This command uses the following syntax:

```
unsetenv <variable>
```

2.5 exit and quit Commands

The `exit` and `quit` commands exit the Octane_ide environment and return you to the System Maintenance Menu. This command uses the following syntax:

```
exit
```

or

```
quit
```

2.6 list Command

The `list` command displays the main Octane_ide diagnostic commands and their descriptions. This command uses the following syntax:

```
list
```

2.7 version Command

The `version` command displays the current version number of Octane_ide and its image build date. This command uses the following syntax:

```
version
```

2.8 xtalk_nic_probe Command

The `xtalk_nic_probe` command searches (“probes”) for devices on the Xtalk bus, beginning with Xtalk port 0xe and proceeding in descending order through six possible ports to port 0x9. If Octane_ide detects a device, it attempts to read the device NIC to identify it. This command uses the following syntax:

```
xtalk_nic_probe
```

2.9 mg_setport Command

The `mg_setport` command is used to set an Xtalk port that contains a graphics board. This command uses the following syntax:

`mg_setport` *<port number in hex or decimal>*

Chapter 3

IP30 Processor Diagnostics

This Chapter lists the IP30 processor diagnostic tests and illustrates the output of a sample test session that uses them.

3.1 Number-in-a-Can Test (NIC)

The NIC diagnostic verifies that no system NIC is missing. NICs are located on the CPU, system board, front plane, and power supplies.

3.2 Heart Test

This diagnostic verifies correct operation of the heart registers by writing data into the registers, reading it back, and comparing the two data patterns. If the heart test fails, replace the IP30 board.

3.3 Bridge Test

This diagnostic verifies correct operation of the bridge registers by writing data into the registers, reading it back, and comparing the two data patterns. If the bridge test fails, replace the IP30 board.

3.4 XBOW Test

This diagnostic verifies correct operation of the XBOW registers by writing data into the registers, reading it back, and comparing the two data patterns. If the XBOW test fails, replace the front plane.

3.5 Memory Test

This diagnostic tests low DRAM (0- to 16-Mbytes) and onboard DRAM (memory above low DRAM). Single-bit and double-bit error detection is tested by inducing spurious errors in the system. If the memory test fails, replace the single in-line memory module (SIMM) that is identified in the error message.

3.6 Built-in Audio Test (RAD)

This diagnostic tests the registers, DMA circuits, and RAM on the audio boards It does not test or verify Radical Audio components. If the RAD test fails, replace the IP30 board.

3.7 IOC3 Test

This diagnostic verifies correct operation of the IOC3 registers by writing data into the registers, reading it back, and comparing the two data patterns. IOC3 also performs an internal Ethernet loopback test and a test of the IOC3 synchronous static random access memory (SSRAM). If the IOC3 test fails, replace the IP30 board.

3.8 Realtime Clock Test (RTC)

This diagnostic verifies correct operation of the realtime clock registers by writing data into the registers, reading it back, and comparing the two data patterns. If the RTC test fails, replace the IP30 board.

3.9 Dual Universal Asynchronous Receiver/Transmitter Test (DUART)

This diagnostic verifies correct operation of the DUART registers by writing data into the registers, reading it back, and comparing the two data patterns. If the DUART test fails, replace the IP30 board.

3.10 Output of a Sample Test Session

```
ide>> ip30


Starting IP30 Tests **********
Number-In-a-Can (NIC) test.

CPU Module NIC:

    Part: 030-0888-004  Name: PM10  Serial: DTT551  Revision: B
      Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000000f07e4



System Board NIC:

    Part: 030-0887-003  Name: IP30  Serial: DRC525  Revision: F
      Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000000ce351



Front Plane NIC:

    Part: 030-0891-003  Name: FP1  Serial: DJH344  Revision: A
      Group: ff  Capability: ffffffff  Variety: ff  Laser: 00000015adf8
    Part: 060-0038-001  Name: PWR.SPPLY.S2  Serial: AAC7400026  Revision: C
      Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000001b22b1



Power Supply NIC:

    Part: 030-0891-003  Name: FP1  Serial: DJH344  Revision: A
      Group: ff  Capability: ffffffff  Variety: ff  Laser: 00000015adf8
    Part: 060-0038-001  Name: PWR.SPPLY.S2  Serial: AAC7400026  Revision: c
      Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000001b22b1



The ethernet NIC was read correctly

Test completed with no errors.

Starting HEART Tests **********
Misc heart register info:
         widget revision number 4
         widget part number 0xc001
         widget manufacturer number 54
     Heart Read-Write Register Test passed.
Heart Miscellaneous Registers Test... Processor ID is 0x0
     Heart Miscellaneous Registers Test passed.
     Heart Interrupt Registers Test passed.
     Heart PIO Access Test passed.
Heart PIU Access Tests... FYI Heart mode 0xe92000000203fdff
     Heart PIU Access Test passed.
HEART Tests Passed **********
```

```
Starting BRIDGE Tests **********
Testing Bridge at xbow port 0xf, addr 0x900000001f000000
Misc bridge register info:
         slot 2 and 4 are not tested as IOC3 uses them
         widget revision number 3
         widget part number 0xc002
         widget manufacturer number 54
         bridge widget interrupt (in heart) 57
     Bridge Read-Write Register Test passed.
     Bridge Interrupt Test passed.
     Bridge Error Test passed.
Bridge RAM test... Testing INTERNAL_ATE RAM as a Bridge RAM
Bridge RAM test... Testing INTERNAL_ATE RAM as a Bridge RAM
Bridge RAM test... Testing EXTERNAL_SYNC SSRAM as a Bridge RAM
                 *** RAM is size 0: not tested ***
     Bridge Bridge Internal/External RAM Test passed.
BRIDGE Tests Passed **********

Starting XBOW Tests **********
Misc xbow register info:
         widget revision number 3
         widget 8 present & alive
         widget c present & alive
         widget f present & alive
     Xbow Read-Write Register Test passed.
Xbow Access Tests... FYI Xbow intr vector 58
Xbow Access Tests...Testing XBOW_WID_ID,  Wr
Xbow Access Tests...Testing XBOW_WID_UNDEF,  Rd
Xbow Access Tests...Testing XBOW_WID_UNDEF,  Wr
     Xbow Access Test passed.
XBOW Tests Passed **********

Starting MEMORY Tests **********
PLEASE WAIT ... THE FOLLOWING TEST TAKES ABOUT 6 MINUTES
parallel execution mode
Low DRAM (0-16MB) address/data bit Test
Testing 16-22MB (scratch area)...
Testing 8-14MB (ide location)...
Testing 0x9000000000000000...
Testing 0x9000000020004000...
Testing 0x9000000020400000...
Testing 0x9000000020e00000...
Test completed with no errors.
vid 0       PASSED
From shortest to longest:
--AddrUniq=0, Kh=1, FastTest=2, MarchY=3, MarchX=4,
--Mats=5, Butterfly=6, AltAccess=7, March=8, WalkingBit=9
--no argument = Addruniq & WalkingBit
Patterns Test, Base: 0x9000000021000000, Size: 0x7000000 bytes
Patterns_l( 9000000021000000, 9000000027ffffff)
     Memory Test passed.
ECC Test

ECC test: sdl/sdr test
```

```
ECC test: error generation
14 base patterns
         base pattern = 0xffffffffffffffff
         base pattern = 0xffffffff00000000
         base pattern = 0xffff0000ffff0000
         base pattern = 0xff00ff00ff00ff00
         base pattern = 0xf0f0f0f0f0f0f0f0
         base pattern = 0xcccccccccccccccc
         base pattern = 0xaaaaaaaaaaaaaaaa
         base pattern = 0x5555555555555555
         base pattern = 0x3333333333333333
         base pattern = 0x0f0f0f0f0f0f0f0f
         base pattern = 0x00ff00ff00ff00ff
         base pattern = 0x0000ffff0000ffff
         base pattern = 0x00000000ffffffff
         base pattern = 0x0000000000000000
heart ecc test: 14 patterns checked, 0 errors

     ECC Test passed.
MEMORY Tests Passed **********


Starting RAD Tests **********
Testing RAD Registers at CONF Addr 0x1f023000, MEM Addr 0x1f700000
     RAD Configuration Space Test passed.
Testing RAD DMA at CONF Addr 0x1f023000, MEM Addr 0x1f700000
     RAD Status DMA Test passed.
Testing RAD RAM at CONF Addr 0x1f023000, MEM Addr 0x1f700000
     RAD RAM Test passed.
RAD Tests Passed **********

Starting IOC3 Tests **********
IOC3 Register Test
     IOC3 Read-Write Register Test passed.
Testing ioc3_sram ....
     IOC3 SRAM Test passed.
Testing ENET TX_CLK  ....
Testing ENET TX_CLK passed
Testing ethernet MAC address NIC  ....
Testing ethernet MAC address NIC passed
Testing ethernet PHY chip registers ....
Testing ethernet PHY chip registers passed
Testing IOC3 internal ethernet loopback ....
   enet_loop: Testing IOC3 LOOPBACK at 100Mb/s.
IOC3 LOOPBACK test passed
Testing PHY chip internal ethernet loopback ....
   enet_loop: Testing PHY LOOPBACK at 10Mb/s.
   enet_loop: Testing PHY LOOPBACK at 100Mb/s.
PHY LOOPBACK test passed
     ENET Tests Test passed.
IOC3 Tests Passed **********

Starting RTC Tests **********
RTC_regs test
     RTC Read-Write Register Test passed.
Starting RTC Functional Tests
Battery voltage check
```

```
RTC Timer Test
RTC NVRAM Test
     PCI Real Time Clock Test passed.
RTC Tests Passed **********

Starting DUART Tests **********
DUART_regs test
     IOC3 DUART Read-Write Register Test passed.
DUART Tests Passed **********
IP30 Tests Passed **********
```

Chapter 4

Processor Module Diagnostics

This Chapter lists the processor module diagnostic tests and illustrates the output of a sample test session that uses them.

4.1 Number-in-a-Can Test (NIC)

This diagnostic verifies that no system NIC is missing. NICs are located on the CPU, system board, front plane, and power supplies.

4.2 Translation Lookaside Buffer Tests (TLB)

Various tests verify the functionality of the TLB.

4.3 Cache Tests

The following tests verify the functionality of the various system caches:

- Data cache data parity test
- Instruction cache data parity test
- Secondary cache ECC (error checking and correction) RAM / Interrupt test
- Secondary cache data and address tests

4.4 Floating-point Unit Tests (FPU)

The following tests verify the functionality of the floating-point unit:

- Control register
- Single-precision addition and subtraction
- Double-precision addition and subtraction
- Single-precision multiplication and subtraction
- Double-precision multiplication and subtraction
- Single-precision multiplication and division
- Double-precision multiplication and division and division by zero
- Inexact result
- Invalid result
- Overflow result
- Underflow result
- Infinite series

4.5 lpackd Test

This diagnostic calculates a linear equation and then a residual to verify the functionality of the FPU.

4.6 Output of a Sample Test Session

```
ide>> pm

Starting PM Tests **********
Number-In-a-Can (NIC) test.

CPU Module NIC:

    Part: 030-0888-004  Name: PM10  Serial: DTT551  Revision: B
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000000f07e4



System Board NIC:

    Part: 030-0887-003  Name: IP30  Serial: DRC525  Revision: F
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000000ce351
```

```
Front Plane NIC:

    Part: 030-0891-003  Name: FP1  Serial: DJH344  Revision: A
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 00000015adf8
    Part: 060-0038-001  Name: PWR.SPPLY.S2  Serial: AAC7400026  Revision: C
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000001b22b1



Power Supply NIC:

    Part: 030-0891-003  Name: FP1  Serial: DJH344  Revision: A
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 00000015adf8
    Part: 060-0038-001  Name: PWR.SPPLY.S2  Serial: AAC7400026  Revision: C
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000001b22b1



The ethernet NIC was read correctly

Test completed with no errors.
[CPU 0] Translation Lookaside Buffer (TLB) test
Test completed with no errors.
[CPU 0] Translation Lookaside Buffer Exception (UTLB) test
Test completed with no errors.
[CPU 0] Data cache data parity test
Test completed with no errors.
[CPU 0] Instruction cache data parity test
Test completed with no errors.
The Icache Test Could Take About 5 minutes... Please wait
[CPU 0] Instruction cache misc tests
Test completed with no errors.
[CPU 0] Secondary Cache ECC RAM/Interrupt Test
Test completed with no errors.
[CPU 0] Secondary cache data and address tests
Test completed with no errors.
[CPU 0] Floating point unit test
Test completed with no errors.
[CPU 0] lpackd test
[CPU 0] lpackd test passed
PM Tests Passed **********
```

Chapter 5

Front Plane Tests (fp)

This Chapter describes the front plane diagnostic test procedure and illustrates the output of a sample test session.

5.1 XBOW Test

This diagnostic verifies correct operation of the XBOW registers by writing data into the registers, reading it back, and comparing the two data patterns. If the XBOW test fails, replace the front plane.

5.2 Output of a Sample Test Session

```
ide>> fp

Starting FRONT PLANE Tests **********

Starting XBOW Tests **********
Misc xbow register info:
         widget revision number 3
         widget 8 present & alive
         widget c present & alive
         widget f present & alive
     Xbow Read-Write Register Test passed.
Xbow Access Tests... FYI Xbow intr vector 58
Xbow Access Tests...Testing XBOW_WID_ID,  Wr
Xbow Access Tests...Testing XBOW_WID_UNDEF,  Rd
Xbow Access Tests...Testing XBOW_WID_UNDEF,  Wr
     Xbow Access Test passed.
XBOW Tests Passed **********
FRONT PLANE Tests Passed **********
```

Chapter 6

Racer Diagnostic

The racer diagnostic is a suite of tests, which includes testing the front plane, processor module, and IP30.

To troubleshoot a failure in the racer diagnostic suite, refer to the section of this document that describes the test that detected the failure.

6.1 Output of a Sample Test Session

```
ide>> racer

Starting PM Tests **********
Number-In-a-Can (NIC) test.

CPU Module NIC:

    Part: 030-0888-004  Name: PM10  Serial: DTT551  Revision: B
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000000f07e4


System Board NIC:

    Part: 030-0887-003  Name: IP30  Serial: DRC525  Revision: F
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000000ce351


Front Plane NIC:

    Part: 030-0891-003  Name: FP1  Serial: DJH344  Revision: A
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 00000015adf8
    Part: 060-0038-001  Name: PWR.SPPLY.S2  Serial: AAC7400026 Revision: C
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000001b22b1


Power Supply NIC:

    Part: 030-0891-003  Name: FP1  Serial: DJH344  Revision: A
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 00000015adf8
    Part: 060-0038-001  Name: PWR.SPPLY.S2  Serial: AAC7400026 Revision: C
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000001b22b1
```

```
The ethernet NIC was read correctly

Test completed with no errors.
[CPU 0] Translation Lookaside Buffer (TLB) test
Test completed with no errors.
[CPU 0] Translation Lookaside Buffer Exception (UTLB) test
Test completed with no errors.
[CPU 0] Data cache data parity test
Test completed with no errors.
[CPU 0] Instruction cache data parity test
Test completed with no errors.
The Icache Test Could Take About 5 minutes... Please wait
[CPU 0] Instruction cache misc tests
Test completed with no errors.
[CPU 0] Secondary Cache ECC RAM/Interrupt Test
Test completed with no errors.
[CPU 0] Secondary cache data and address tests
Test completed with no errors.
[CPU 0] Floating point unit test
Test completed with no errors.
[CPU 0] lpackd test
[CPU 0] lpackd test passed
PM Tests Passed **********


Starting FRONT PLANE Tests **********

Starting XBOW Tests **********
Misc xbow register info:
         widget revision number 3
         widget 8 present & alive
         widget c present & alive
         widget f present & alive
     Xbow Read-Write Register Test passed.
Xbow Access Tests... FYI Xbow intr vector 58
Xbow Access Tests...Testing XBOW_WID_ID,  Wr
Xbow Access Tests...Testing XBOW_WID_UNDEF,  Rd
Xbow Access Tests...Testing XBOW_WID_UNDEF,  Wr
     Xbow Access Test passed.
XBOW Tests Passed **********
FRONT PLANE Tests Passed **********


Starting IP30 Tests **********
Number-In-a-Can (NIC) test.

CPU Module NIC:

    Part: 030-0888-004  Name: PM10  Serial: DTT551  Revision: B
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000000f07e4


System Board NIC:

    Part: 030-0887-003  Name: IP30  Serial: DRC525  Revision: F
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000000ce351
```

```
Front Plane NIC:

    Part: 030-0891-003  Name: FP1  Serial: DJH344  Revision: A
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 00000015adf8
    Part: 060-0038-001  Name: PWR.SPPLY.S2  Serial: AAC7400026 Revision: C
       Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000001b22b1



Power Supply NIC:

      Part: 030-0891-003  Name: FP1  Serial: DJH344  Revision: A
         Group: ff  Capability: ffffffff  Variety: ff  Laser:
00000015adf8
      Part: 060-0038-001  Name: PWR.SPPLY.S2  Serial: AAC7400026
Revision: C
         Group: ff  Capability: ffffffff  Variety: ff  Laser:
0000001b22b1



The ethernet NIC was read correctly

Test completed with no errors.

Starting HEART Tests **********
Misc heart register info:
         widget revision number 4
         widget part number 0xc001
         widget manufacturer number 54
     Heart Read-Write Register Test passed.
Heart Miscellaneous Registers Test... Processor ID is 0x0
     Heart Miscellaneous Registers Test passed.
     Heart Interrupt Registers Test passed.
     Heart PIO Access Test passed.
Heart PIU Access Tests... FYI Heart mode 0xe92000000203fdff
     Heart PIU Access Test passed.
HEART Tests Passed **********

Starting BRIDGE Tests **********
Testing Bridge at xbow port 0xf, addr 0x900000001f000000
Misc bridge register info:
         slot 2 and 4 are not tested as IOC3 uses them
         widget revision number 3
         widget part number 0xc002
         widget manufacturer number 54
         bridge widget interrupt (in heart) 57
     Bridge Read-Write Register Test passed.
     Bridge Interrupt Test passed.
     Bridge Error Test passed.
Bridge RAM test... Testing INTERNAL_ATE RAM as a Bridge RAM
Bridge RAM test... Testing INTERNAL_ATE RAM as a Bridge RAM
Bridge RAM test... Testing EXTERNAL_SYNC SSRAM as a Bridge RAM
                 *** RAM is size 0: not tested ***
     Bridge Bridge Internal/External RAM Test passed.
BRIDGE Tests Passed **********
```

```
Starting XBOW Tests **********
Misc xbow register info:
         widget revision number 3
         widget 8 present & alive
         widget c present & alive
         widget f present & alive
     Xbow Read-Write Register Test passed.
Xbow Access Tests... FYI Xbow intr vector 58
Xbow Access Tests...Testing XBOW_WID_ID,  Wr
Xbow Access Tests...Testing XBOW_WID_UNDEF,  Rd
Xbow Access Tests...Testing XBOW_WID_UNDEF,  Wr
     Xbow Access Test passed.
XBOW Tests Passed **********

Starting MEMORY Tests **********
PLEASE WAIT ... THE FOLLOWING TEST TAKES ABOUT 6 MINUTES
parallel execution mode
Low DRAM (0-16MB) address/data bit Test
Testing 16-22MB (scratch area)...
Testing 8-14MB (ide location)...
Testing 0x9000000000000000...
Testing 0x9000000020004000...
Testing 0x9000000020400000...
Testing 0x9000000020e00000...
Test completed with no errors.
vid 0       PASSED
>From shortest to longest:
--AddrUniq=0, Kh=1, FastTest=2, MarchY=3, MarchX=4,
--Mats=5, Butterfly=6, AltAccess=7, March=8, WalkingBit=9
--no argument = Addruniq & WalkingBit
Patterns Test, Base: 0x9000000021000000, Size: 0x7000000 bytes
Patterns_l( 9000000021000000, 9000000027ffffff)
     Memory Test passed.
ECC Test

ECC test: sdl/sdr test

ECC test: error generation
14 base patterns
         base pattern = 0xffffffffffffffff
         base pattern = 0xffffffff00000000
         base pattern = 0xffff0000ffff0000
         base pattern = 0xff00ff00ff00ff00
         base pattern = 0xf0f0f0f0f0f0f0f0
         base pattern = 0xcccccccccccccccc
         base pattern = 0xaaaaaaaaaaaaaaaa
         base pattern = 0x5555555555555555
         base pattern = 0x3333333333333333
         base pattern = 0x0f0f0f0f0f0f0f0f
         base pattern = 0x00ff00ff00ff00ff
         base pattern = 0x0000ffff0000ffff
         base pattern = 0x00000000ffffffff
         base pattern = 0x0000000000000000
heart ecc test: 14 patterns checked, 0 errors

     ECC Test passed.
MEMORY Tests Passed **********
```

```
Starting RAD Tests **********
Testing RAD Registers at CONF Addr 0x1f023000, MEM Addr 0x1f700000
     RAD Configuration Space Test passed.
Testing RAD DMA at CONF Addr 0x1f023000, MEM Addr 0x1f700000
     RAD Status DMA Test passed.
Testing RAD RAM at CONF Addr 0x1f023000, MEM Addr 0x1f700000
     RAD RAM Test passed.
RAD Tests Passed **********

Starting IOC3 Tests **********
IOC3 Register Test
     IOC3 Read-Write Register Test passed.
Testing ioc3_sram ....
     IOC3 SRAM Test passed.
Testing ENET TX_CLK  ....
Testing ENET TX_CLK passed
Testing ethernet MAC address NIC  ....
Testing ethernet MAC address NIC passed
Testing ethernet PHY chip registers ....
Testing ethernet PHY chip registers passed
Testing IOC3 internal ethernet loopback ....
   enet_loop: Testing IOC3 LOOPBACK at 100Mb/s.
IOC3 LOOPBACK test passed
Testing PHY chip internal ethernet loopback ....
   enet_loop: Testing PHY LOOPBACK at 10Mb/s.
   enet_loop: Testing PHY LOOPBACK at 100Mb/s.
PHY LOOPBACK test passed
     ENET Tests Test passed.
IOC3 Tests Passed **********

Starting RTC Tests **********
RTC_regs test
     RTC Read-Write Register Test passed.
Starting RTC Functional Tests
Battery voltage check
RTC Timer Test
RTC NVRAM Test
     PCI Real Time Clock Test passed.
RTC Tests Passed **********

Starting DUART Tests **********
DUART_regs test
     IOC3 DUART Read-Write Register Test passed.
DUART Tests Passed **********
IP30 Tests Passed **********

ALL TESTS IN RACER Passed **********
```

Chapter 7

Graphics Board Diagnostic

The Octane_ide graphics test (gfx) verifies the connectivity and functionality of the components on the graphics board. If an error is detected, the test stops and displays the error. Normally, to correct a gfx failure, you should replace the graphics board.

7.1 List of Tests Run by gfx in Sequence Order

7.1.1 HQ Tests

The HQ tests verify Xtalk bus connectivity and the internal functionality of the HQ and its registers.

7.1.2 NIC Test

The NIC test verifies the contents of the graphics board NIC.

7.1.3 HQ Realtime Path Test

The HQ Realtime (RT) Path test verifies the functionality of the realtime video control path.

7.1.4 RSS Bus Test

The RSS bus test verifies the functionality of the HQ-RE-GE bus.

7.1.5 Display Backend Tests

The Display Backend tests verify the functionality of various graphics components such as the digital-to-analog converter (DAC), color map (CMAP), video timing tables, windows map (XMAP), registers, and cursor.

7.1.6 GE Tests

The GE tests verify the functionality of the geometry engine application-specific integrated circuit (ASIC), including the microcode, internal and external random access memory (RAM), arithmetic and logic unit (ALU), registers, instructions, and direct memory access (DMA).

7.1.7 RE Tests

The RE tests verify the functionality of the raster engine ASIC, including register reads and writes and the internal RAM.

7.1.8 RDRAM Test

The RDRAM tests verify the functionality of the graphics framebuffer memory (RDRAM, a high bandwidth DRAM, designed by Rambus Inc. of Mountain View, CA).

7.1.9 RE/PP Tests

The RE / PP tests verify the rendering functionality of the RE and PP (pixel processor) ASICs by drawing and confirming the accuracy of a series of images.

7.1.10 TE/TRAM Tests

The TE / TRAM tests verify the functionality of the texture engine (TE) and the texture RAM (TRAM) ASICs by performing register reads and writes, TRAM memory tests, and texture rendering tests.

You can run these tests manually by entering `mg_test_tram`; however, these tests always run automatically as part of gfx if Octance_ide detects texturing hardware on the graphics board.

7.2 Testing Systems with Multiple Graphics Boards

If an OCTANE system contains two graphics boards, gfx and mg_test_tram, by default, test the board with the lower Xtalk port number.

To test the second board, you must determine its Xtalk port number using one of the following procedures:

- At the Command Monitor, issue the `system` command.
- At IDE, issue the `xtalk_nic_probe` command.
- At the IRIX operating system, issue the `find` command.

7.2.1 Determining the Xtalk Port Number with the Command Monitor

At the Command Monitor prompt, enter the following command:

```
>> system

IP30 system:
   CPU speed ~195Mhz
   Cache speed divisor 1.5
   SysAD speed divisor 2
   4 outstanding read(s)
   R10K Revision: 2.7
   Password jumper on
   Number of XIO fan loads 0 (0,env=unset)
Chips/NICs:
   heart(rev D):
      Part: 030-0888-004  Name: PM10  Serial: DTT551
        Revision: B  Group: ff  Capability: ffffffff
        Variety: ff  Laser: 0000000f07e4
   xbow(rev 1.2):
   bridge(rev C):
      Part: 030-0887-003  Name: IP30  Serial: DRC525
        Revision: F  Group: ff  Capability: ffffffff
        Variety: ff  Laser: 0000000ce351
   ioc3(rev 1): eaddr 08:00:69:0a:2d:34
      Part: 030-0891-003  Name: FP1  Serial: DJH344
        Revision: A  Group: ff  Capability: ffffffff
        Variety: ff  Laser: 00000015adf8
      Part: 060-0038-001  Name: PWR.SPPLY.S2  Serial: AAC7400026
        Revision: C  Group: ff  Capability: ffffffff
        Variety: ff  Laser: 0000001b22b1
   xtalk 0xc HQ4:
      Part: 030-0938-003  Name: GM10  Serial: EBR620
        Revision: M  Group: ff  Capability: ffffffff
        Variety: ff  Laser: 0000000cda9f
   xtalk 0xb HQ4:
      Part: 030-0957-003  Name: GM20  Serial: DZD021
        Revision: M  Group: ff  Capability: ffffffff
        Variety: ff  Laser: 0000001abbb9
```

Determine which Xtalk devices are active within the “Chips / NICs” section. Refer to the following example:

```
xtalk 0xc HQ4:
      Part: 030-0938-003  Name: GM10  Serial: EBR620
        Revision: M  Group: ff  Capability: ffffffff
        Variety: ff  Laser: 0000000cda9f
xtalk 0xb HQ4:
      Part: 030-0957-003  Name: GM20  Serial: DZD021
        Revision: M  Group: ff  Capability: ffffffff
        Variety: ff  Laser: 0000001abbb9
```

Two devices are listed. One device is the GM10, which is an SI graphics board. The other is a GM20, which is an MXI board. You can find the port number for each device on the first line of its output, directly to the right of the word *xtalk*. In the example above, the port numbers are 0xc for the GM10 and 0xb for the GM20.

With that information, enter `mg_setport` in Origin_ide to select the graphics board to test.

```
ide>> mg_setport 0xc
 port set to 12
```

7.2.2 Determining the Xtalk Port Number with IDE

Use the *xtalk_nic_probe* command to probe for devices on the Xtalk bus. The probe begins at Xtalk port 0xe and proceeds in descending order through the 6 possible ports to port 0x9. If IDE detects a device, it attempts to read the NIC of the device to determine what kind of device it has detected.

```
ide>> xtalk_nic_probe

No device seen at port 0xe
No device seen at port 0xd

Part: 030-0957-003  Name: GM20  Serial: DZD021  Revision: N
   Group: ff  Capability: ffffffff Variety: ff  Laser: 000001abbb9

Part: 030-0938-003  Name: GM10  Serial: EBR551  Revision: N
   Group: ff  Capability: ffffffff Variety: ff  Laser: 000000cdc1b
No device seen at port 0xa
No device seen at port 0x9
```

In this example, no devices are detected at ports 0xe, 0xd, 0xa, and 0x9. Ports 0xb and 0xc each contain a device: a GM10 graphics board on Port 0xb and a GM20 graphics board on Port 0xc.

Having that information, enter `mg_setport` within Octane_ide to specify which graphics board to test.

```
ide>> mg_setport 0xc
 port set to 12
```

7.2.3 Determining the Xtalk Port Number with the IRIX Operating System

To find the Xtalk port numbers of the graphics cards in IRIX, examine the hardware graph by entering the `find` command to search for the word *mgras*:

```
# find /hw -name mgras -print
/hw/node/xtalk/12/mgras
/hw/node/xtalk/11/mgras
```

The response indicates that two boards were found. The first board is located at port 0xc (12 decimal) and the second at 0xb (11 decimal).

With that information, enter the command `mg_setport` within Octane_ide to specify which graphics board to test.

```
ide>> mg_setport 0xc
 port set to 12
```

7.3 Output of a Sample Test Session

```
ide>> gfx
 Iteration  1
 GAMERA found in port 0xc
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
Loading Cmaps with a Linear Ramp
Loading Gamma Tables with a Linear Ramp

Starting HQ Tests **********
 GAMERA found in port 0xc
MGRAS HQ XIO Bus Test
     HQ XIO Bus Test passed.
HQ DCB Ctrl Test
     HQ DCB Ctrl Test passed.
HQ TLB Test
     HQ TLB Test passed.
HQ reif_ctx Register test
     HQ REIF CTX Test passed.
MGRAS HQ Hag_ctx Register test
     HQ HAG CTX Test passed.
MGRAS HQ Ucode RAM test
     HQ Ucode DataBus Test passed.
     HQ Ucode AddrBus Test passed.
     HQ Ucode AddrUniquness Test passed.
     HQ Ucode Pattern Test passed.
 GAMERA found in port 0xc

HQ ucode download was successful -- no errors detected
HQ_CP test - cp_dmove12_1:
HQ_CP test - cp_dmove12_1: passed
HQ_CP test - cp_dmove12_2:
HQ_CP test - cp_dmove12_2: passed
HQ_CP test - cp_dmove12_3:
HQ_CP test - cp_dmove12_3: passed
HQ_CP test - cp_imove1:
HQ_CP test - cp_imove1: passed
HQ_CP test - cp_imove2:
HQ_CP test - cp_imove2: passed
HQ_CP test - cp_mix1:
HQ_CP test - cp_mix1: passed
HQ_CP test - cp_mix2:
HQ_CP test - cp_mix2: passed
     HQ CP_Functionality Test passed.
```

```
HQ ucode download was successful -- no errors detected
     HQ Converter 32-bit Test passed.
     HQ Converter 16-bit Test passed.
     HQ Converter 8-bit Test Test passed.
     HQ Convert Stuff Test Test passed.
Mgras HQ3 Converter Test passed

HQ ucode download was successful -- no errors detected
     HQ CFIFO Functionality Test passed.
     HQ4 Register Test Test passed.
HQ Tests Passed **********

      Part: 030-0938-003  Name: GM10  Serial: EBR620  Revision: M
        Group: ff  Capability: ffffffff  Variety: ff  Laser: 0000000cda9f


 GAMERA found in port 0xc
 ============  Data Format tests done through PIO =============
 PIO Diag Mode Passed in TEX_RGBA16_IN and TEX_RGBA12_OUT
 PIO Diag Mode Passed in TEX_RGBA16_IN and TEX_RGBA8_OUT
 PIO Diag Mode Passed in TEX_SHORT_IN and TEX_SHORT_OUT
 PIO Diag Mode Passed in TEX_RGBA10_IN and TEX_RGBA12_OUT
 PIO Diag Mode Passed in TEX_RGBA10_IN and TEX_RGBA8_OUT
 PIO Diag Mode Passed in TEX_ABGR8_IN and TEX_RGBA12_OUT
 PIO Diag Mode Passed in TEX_ABGR8_IN and TEX_RGBA8_OUT
 PIO Diag Mode Passed in TEX_RGBA8_IN and TEX_RGBA12_OUT
 PIO Diag Mode Passed in TEX_RGBA8_IN and TEX_RGBA8_OUT
 GAMERA found in port 0xc
 Real Time DMA diag mode Passed

Starting RSSBUS Tests **********
Testing RSS-0
     HQ HQ_RSS_DataBus Test passed.
RSSBUS Tests Passed **********
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
Loading Cmaps with a Linear Ramp
Loading Gamma Tables with a Linear Ramp

Starting BACK_END Tests **********
 GAMERA found in port 0xc

Starting DAC Tests **********
DAC Mode Register Test
     DAC Mode Reg Test passed.
DAC Address Register Test
     DAC Addr Reg Test passed.
Color Palette Address Uniquness Test
     DAC Color Palette Addr Uniq Test passed.
Color Palette Walking Bit: DataBus Test
     DAC Color Palette Addr Bus Test passed.
Color Pallette Pattern Test
     DAC Color Palette Patrn Test passed.
DAC Tests Passed **********
```

```
Starting VC3 Tests **********
VC3 Internal Register Test
     VC3 Register Test passed.
VC3 SRAM Address Bus: Walking Ones & Zeros Test
     VC3 Address Bus Test passed.
VC3 SRAM Data Bus: Walking Ones & Zeros Test
     VC3 Data Bus Test passed.
VC3 SRAM Address Uniqueness Test
     VC3 Address Uniqness Test passed.
VC3 SRAM Pattern Test
     VC3 Pattern Test passed.
VC3 Tests Passed **********

Starting CMAP Tests **********
CMAP0 data bus test
     Cmap0 Data Bus Test passed.
CMAP 0 Address Bus Test
     Cmap0 Address Bus Test passed.
saddr 0 eaddr 8191
CMAP0 Pattern Test
Loop 0 Writing Pattern
0x5a5a5a5a 0x3c3c3c3c 0xfffffffff0f0f0f0 0xffffffffa5a5a5a5
0xffffffffc3c3c3c3 0xf0f0f0f
Loop 1 Writing Pattern
0x3c3c3c3c 0xfffffffff0f0f0f0 0xffffffffa5a5a5a5 0xffffffffc3c3c3c3
0xf0f0f0f 0x5a5a5a5a
Loop 2 Writing Pattern
0xfffffffff0f0f0f0 0xffffffffa5a5a5a5 0xffffffffc3c3c3c3 0xf0f0f0f
0x5a5a5a5a 0x3c3c3c3c
Loop 3 Writing Pattern
0xffffffffa5a5a5a5 0xffffffffc3c3c3c3 0xf0f0f0f 0x5a5a5a5a 0x3c3c3c3c
0xfffffffff0f0f0f0
Loop 4 Writing Pattern
0xffffffffc3c3c3c3 0xf0f0f0f 0x5a5a5a5a 0x3c3c3c3c 0xfffffffff0f0f0f0
0xffffffffa5a5a5a5
Loop 5 Writing Pattern
0xf0f0f0f 0x5a5a5a5a 0x3c3c3c3c 0xfffffffff0f0f0f0 0xffffffffa5a5a5a5
0xffffffffc3c3c3c3
     Cmap0 Pattern Test passed.
CMAP0 Address Uniqueness Test
     Cmap0 Address Uniqness Test passed.
CMAP1 data bus test
     Cmap1 Data Bus Test passed.
CMAP 1 Address Bus Test
     Cmap1 Address Bus Test passed.
saddr 0 eaddr 8191
CMAP1 Pattern Test
Loop 0 Writing Pattern
0x5a5a5a5a 0x3c3c3c3c 0xfffffffff0f0f0f0 0xffffffffa5a5a5a5
0xffffffffc3c3c3c3 0xf0f0f0f
Loop 1 Writing Pattern
0x3c3c3c3c 0xfffffffff0f0f0f0 0xffffffffa5a5a5a5 0xffffffffc3c3c3c3
0xf0f0f0f 0x5a5a5a5a
Loop 2 Writing Pattern
0xfffffffff0f0f0f0 0xffffffffa5a5a5a5 0xffffffffc3c3c3c3 0xf0f0f0f
0x5a5a5a5a 0x3c3c3c3c
Loop 3 Writing Pattern
```

```
0xffffffffa5a5a5a5 0xffffffffc3c3c3c3 0xf0f0f0f0 0x5a5a5a5a 0x3c3c3c3c
0xfffffffff0f0f0f0
Loop 4 Writing Pattern
0xffffffffc3c3c3c3 0xf0f0f0f0 0x5a5a5a5a 0x3c3c3c3c 0xfffffffff0f0f0f0
0xffffffffa5a5a5a5
Loop 5 Writing Pattern
0xf0f0f0f0 0x5a5a5a5a 0x3c3c3c3c 0xfffffffff0f0f0f0 0xffffffffa5a5a5a5
0xffffffffc3c3c3c3
     Cmap1 Pattern Test passed.
CMAP1 Address Uniqueness Test
     Cmap1 Address Uniqness Test passed.
CMAP Tests Passed **********
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
Loading Cmaps with a Linear Ramp
Loading Gamma Tables with a Linear Ramp
 GAMERA found in port 0xc
_mgras_dcbdma_enabled 0x1
Enabled DCB-DMA

Starting DAC Tests in DCBDMA Mode **********

Starting DAC Tests **********
DAC Mode Register Test
     DAC Mode Reg Test passed.
DAC Address Register Test
     DAC Addr Reg Test passed.
Color Palette Address Uniquness Test
     DAC Color Palette Addr Uniq Test passed.
Color Palette Walking Bit: DataBus Test
     DAC Color Palette Addr Bus Test passed.
Color Pallette Pattern Test
     DAC Color Palette Patrn Test passed.
DAC Tests Passed **********
DAC Tests in DCBDMA Mode Passed **********

Starting VC3 Tests in DCBDMA Mode **********

Starting VC3 Tests **********
VC3 Internal Register Test
     VC3 Register Test passed.
VC3 SRAM Address Bus: Walking Ones & Zeros Test
     VC3 Address Bus Test passed.
VC3 SRAM Data Bus: Walking Ones & Zeros Test
     VC3 Data Bus Test passed.
VC3 SRAM Address Uniqueness Test
     VC3 Address Uniqness Test passed.
VC3 SRAM Pattern Test
     VC3 Pattern Test passed.
VC3 Tests Passed **********
VC3 Tests in DCBDMA Mode Passed **********
_mgras_dcbdma_enabled 0x0
Disabled DCB-DMA
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
```

```
Loading Cmaps with a Linear Ramp
Loading Gamma Tables with a Linear Ramp
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
Loading Cmaps with a Linear Ramp
Loading Gamma Tables with a Linear Ramp
MGRAS_XMAP_DCB Register Test
     XMAP0 DCB Reg Test passed.
MGRAS_XMAP_DCB Register Test
     XMAP1 DCB Reg Test passed.
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
Loading Cmaps with a Linear Ramp
Loading Gamma Tables with a Linear Ramp
Started Video Timing
     CRC: Walk One PixelPath Test passed.
     CRC: Walk One PixelPath Test passed.
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
Loading Cmaps with a Linear Ramp
Loading Gamma Tables with a Linear Ramp
Testing 1600x1200 timing
Stopped Video Timing
Started Video Timing
     CRC: Walk One PixelPath Test passed.
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
Loading Cmaps with a Linear Ramp
Loading Gamma Tables with a Linear Ramp
Executing mg_vc3cursorposition test...
BACK_END Tests Passed **********
 I2C 8584 Probing Complete
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
Loading Cmaps with a Linear Ramp
Loading Gamma Tables with a Linear Ramp
1 GE's found in the SYSTEM
Testing 1GE system....
 GAMERA found in port 0xc
1 GE's found in the SYSTEM
------   Executing GE Test Suite on :: GE0       ------
 GAMERA found in port 0xc
1 GE's found in the SYSTEM
testing GE0 Ucode memory....
testing ge0_ucode 1....
 GAMERA found in port 0xc
testing ge0_ucode 2....
testing ge_ucode_test 2....
MGRAS GE11 Ucode Data Bus Test
     GE11 Ucode DataBus Test passed.
testing ge_ucode_test 3....
MGRAS GE11 Ucode Address Bus Test
```

```
     GE11 Ucode AddrBus Test passed.
testing ge_ucode_test 4....
MGRAS GE11 Ucode Address Uniqueness Test
/     GE11 Ucode AddrUniquness Test passed.
testing ge_ucode_test 5....
MGRAS GE11 Ucode Memory Patterns  Test
|     GE11 Ucode Pattern Test passed.
testing ge0_ucode 3....
testing ge0_ucode 3....
testing ge0_setup 1....
 GAMERA found in port 0xc
testing ge0_setup 2....
1 GE's found in the SYSTEM
testing ge0_setup 3....
testing ge0_setup 4....
------   Executing GE0 test setup        ------
 GAMERA found in port 0xc
 GAMERA found in port 0xc
     GE11 Ucode Dnload Test passed.
testing ge0_setup 5....
 GAMERA found in port 0xc
testing getest 1....
 mg_ge_cram in progress
     GE11 cram Test passed.
testing getest 2....
 mg_ge_eram in progress
     GE11 eram Test passed.
testing getest 3....
 mg_ge_wram in progress
     GE11 wram Test passed.
testing getest 4....
 give more delay
testing getest 5....
 mg_ge_alu in progress
     GE11 alu Test passed.
testing getest 6....
 mg_ge_dreg in progress
     GE11 dreg Test passed.
 mg_ge_inst in progress
testing getest 7....
     GE11 inst Test passed.
testing getest 8....
 mg_ge_dma in progress
     GE11 DMA Test passed.
******** GE Test Suite Execution Completed       ********
 GAMERA found in port 0xc
 mgbase before MgrasSyncREPP 0x900000001c000000
 mgbase in the MgrasSyncREPP function 0x900000001c000000
 mgbase after MgrasSyncREPP 0x900000001c000000
 mgbase before MgrasSyncREPP 0x900000001c000000
 mgbase in the MgrasSyncREPP function 0x900000001c000000
 mgbase after MgrasSyncREPP 0x900000001c000000

Starting RE Tests **********
     RE4-0 Status Reg Test passed.
     RE4-0 RdWr Regs Test passed.
RAM KH Test: PASSED
```

```
RAM KH Test: PASSED
RAM KH Test: PASSED
RAM KH Test: PASSED
RAM KH Test: PASSED
RAM KH Test: PASSED
RAM KH Test: PASSED
RAM KH Test: PASSED
RAM KH Test: PASSED
RAM KH Test: PASSED
RAM KH Test: PASSED
RAM March X Test: PASSED
RAM March X Test: PASSED
RAM March X Test: PASSED
RAM March X Test: PASSED
RAM March X Test: PASSED
RAM March X Test: PASSED
RAM March X Test: PASSED
RAM March X Test: PASSED
RAM March X Test: PASSED
RAM March X Test: PASSED
RAM March X Test: PASSED
RAM March Y Test: PASSED
RAM March Y Test: PASSED
RAM March Y Test: PASSED
RAM March Y Test: PASSED
RAM March Y Test: PASSED
RAM March Y Test: PASSED
RAM March Y Test: PASSED
RAM March Y Test: PASSED
RAM March Y Test: PASSED
RAM March Y Test: PASSED
RAM March Y Test: PASSED
RE Tests Passed **********

Starting DMA Tests **********
     HQ HOST->HQ DMA data path Test passed.

HQ ucode download was successful -- no errors detected
     HQ HOST->HQ->CP DMA data path Test passed.
Color Buffer AB DMA Test

     Framebuffer RDRAM (Using DMA style 002) Test passed.
DMA Tests Passed **********

Starting QUICK RDRAM Tests **********
Color Buffer AB DMA Test

     Framebuffer RDRAM (Using DMA style 005) Test passed.
QUICK RDRAM Tests Passed **********

Starting RDRAM Tests **********
Z Buffer DMA Test
Pattern pass 0....
Pattern pass 1....
Pattern pass 2....
Pattern pass 3....
Pattern pass 4....
```

```
Pattern pass 5....
     Framebuffer RDRAM (Using DMA style 005) Test passed.
Color Buffer AB DMA Test
Pattern pass 0....
Pattern pass 1....
Pattern pass 2....
Pattern pass 3....
Pattern pass 4....
Pattern pass 5....
     Framebuffer RDRAM (Using DMA style 005) Test passed.
Overlay Buffer DMA Test
Pattern pass 0....
Pattern pass 1....
Pattern pass 2....
Pattern pass 3....
Pattern pass 4....
Pattern pass 5....
     Framebuffer RDRAM (Using DMA style 005) Test passed.
RDRAM Tests Passed **********

Starting RE-PP Tests **********
 GAMERA found in port 0xc
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
Loading Cmaps with a Linear Ramp
Loading Gamma Tables with a Linear Ramp
 mgbase before MgrasSyncREPP 0x900000001c000000
 mgbase in the MgrasSyncREPP function 0x900000001c000000
 mgbase after MgrasSyncREPP 0x900000001c000000
 mgbase before MgrasSyncREPP 0x900000001c000000
 mgbase in the MgrasSyncREPP function 0x900000001c000000
 mgbase after MgrasSyncREPP 0x900000001c000000
 mg_z_tri in progess ...
     RE4 Z Test passed.
     RE4 Z Test passed.
     RE4 Z Test passed.
 mg_lines in progess ...
     RE4 Line Test passed.
 mg_points in progess ...
     RE4 Points Test passed.
 mg_stip_tri in progess ...
     RE4 PolyStiP Test passed.
 mg_xblock in progress ...
     RE4 Xblk Test passed.
 mg_chars in progress ...
     RE4 Chars Test passed.
 mg_logicop in progress ...
     RSS, PP1, LOGICOP Test passed.
 mg_dither in progress ...
     RSS, PP1, DITHER Test passed.
 mg_color_tri in progress ...
Color Triangle Test: Red Triangle passed
Color Triangle Test: Green Triangle passed
Color Triangle Test: Blue Triangle passed
Color Triangle Test: Alpha Triangle passed
     RE4 Color Tri Test passed.
```

```
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
Loading Cmaps with a Linear Ramp
Loading Gamma Tables with a Linear Ramp
     RE4 Alpha Blend Test passed.
Checking RSS-0 PP0 crc...

alphablend RSS-0 PP0 crc PASSED

Checking RSS-0 PP1 crc...

alphablend RSS-0 PP1 crc PASSED

********  Alphablend Test with DAC CRC PASSED ********
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
Loading Cmaps with a Linear Ramp
Loading Gamma Tables with a Linear Ramp
------    Executing Scene Test with CRC ------
------    Testing the scene in the display buffer ------
Checking RSS-0 PP0 crc...

scene_test display buffer RSS-0 PP0 crc PASSED

Checking RSS-0 PP1 crc...

scene_test display buffer RSS-0 PP1 crc PASSED

------    Testing the scene in the overlay buffer ------
 GAMERA found in port 0xc
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
Loading Cmaps with a Linear Ramp
Loading Gamma Tables with a Linear Ramp
 mgbase before MgrasSyncREPP 0x900000001c000000
 mgbase in the MgrasSyncREPP function 0x900000001c000000
 mgbase after MgrasSyncREPP 0x900000001c000000
 mgbase before MgrasSyncREPP 0x900000001c000000
 mgbase in the MgrasSyncREPP function 0x900000001c000000
 mgbase after MgrasSyncREPP 0x900000001c000000
Checking RSS-0 PP0 crc...

scene_test overlay buffer RSS-0 PP0 crc PASSED

Checking RSS-0 PP1 crc...

scene_test overlay buffer RSS-0 PP1 crc PASSED

Resetting graphics
 GAMERA found in port 0xc
Mgras Initialize
Mgras DacReset
Mgras VC3 Reset
Loading Cmaps with a Linear Ramp
```

```
Loading Gamma Tables with a Linear Ramp
 mgbase before MgrasSyncREPP 0x900000001c000000
 mgbase in the MgrasSyncREPP function 0x900000001c000000
 mgbase after MgrasSyncREPP 0x900000001c000000
 mgbase before MgrasSyncREPP 0x900000001c000000
 mgbase in the MgrasSyncREPP function 0x900000001c000000
 mgbase after MgrasSyncREPP 0x900000001c000000
********  Scene Test with DAC CRC PASSED ********
RE-PP Tests Passed **********
numTRAMs: 0
No Texture Subsystem in the Graphics Board
Tests for Texture Subsystem are skipped...
GRAPHICS Tests Passed **********
ALL TESTS IN GRAPHICS PASSED
```

Chapter 8

Texture RAM Diagnostic

The TE / TRAM tests verify the functionality of the texture engine (TE) and the texture RAM (TRAM) ASICs by performing register reads and writes, TRAM memory tests, and texture rendering tests. Refer to the previous Chapter for additional information.

These tests always run automatically as part of gfx if Octane_ide detects texturing hardware on the graphics board; however, Octane_ide enables you to run these tests manually by entering `mg_test_tram`. For example, you can verify only the texturing hardware when you suspect that the texture mapping function is problematic.

When it detects a failure, TRAM always identifies an OCTANE graphics board (GM10 or GM20) as the faulty FRU, which is not entirely correct. The cause of the failure may actually be one of the TMEZZ cards that are mounted on the graphics board. To correct a gfx or mg_test_tram failure, you should reseat or replace either the graphics board identified in the test results or the TMEZZ cards mounted on the graphics board.

Chapter 9

PCI Shoebox Diagnostic

9.1 PCI Shoebox Diagnostic Description

The PCI Shoebox Diagnostic requires that the OCTANE system contain a PCI Shoebox for it to run correctly. Otherwise, a system exception will result and you will have to reset the system or press enter to return to the system maintenance menu. If the PCI Shoebox test fails, replace the PCI Shoebox.

9.2 Output of a Sample Test Session

```
Starting SHOEBOX test **********
Running All PCI Shoe Box Tests
Testing Bridge at xbow port 0xd, addr 0x900000001d000000
Misc bridge register info:
        slot 2 and 4 are not tested as IOC3 uses them
        widget revision number 3\
        widget part number 0xc002
        widget manufacturer number 54
        bridge widget interrupt ( in hear ) 55
     Bridge Read-Write Register Test passed.
Bridge RAM test... Testing INTERNAL_ATE RAM as a Bridge RAM
Bridge RAM test... Testing INTERNAL_ATE RAM as a Bridge RAM
Bridge RAM test... Testing EXTERNAL_SYNC SSRAM as a Bridge RAM
                *** RAM is size 0: not tested ***
        Bridge Bridge Internal/External RAM Test passed.
        Bridge Error Test passed.
        PCI Shoebox All Test passed.

SHOEBOX test passed
```

Appendix A

Sample Errors and Exception Output

A.1 Sample Output of a Failure Detected by mg_test_ram

The following display indicates that a failure occurred during the mg_test_tram diagnostic. The diagnostic reports that the failing FRU is the GM20 graphics board, which may not be completely accurate. Refer to Chapter 8 for more information on this error.

```
Starting TRAM Tests ******************
numTRAMS : 4

RSS-0, Testing 4 TRAMS.
TRAM Revision register (word 0): 0x1c011401
TRAM Revision register (word 1): 0xc000400

    Texture TRAM (Using DMA style 014) Test passed.

RSS-1, Testing 4 TRAMS.
TRAM Revision register (word 0) : 0x1401
TRAM Revision register (word 1) : 0xc000400
                                       - ERROR -

ERROR***TRAM Revision High Word failed, TRAM-REBus exp: 1c011401, rcv:
1401, diff: 1c010000

                                       - ERROR _
**** Texture TRAM (Using DMA style 014) Test failed. ErrCode DM014
Errors 1
The faulty FRU is GM20
mg_tram_rev_nobuff failed

Failure Detected in TRAM test
```

A.2 Sample Outputs of Failures Detected by gfx

A.2.1 RDRAM Section Error

The following display reports that a failure occured during the RDRAM (Rambus(tm) DRAM) section of the gfx jtest. In this example, the failing FRU is the GM20 graphics board.

```
Starting RDRAM Tests  ***********
Z Buffer DMA Test
Pattern pass 0 .....
Pattern pass 1 ..... Pattern pass 2 ......
Pattern pass 3 .....
Pattern pass 4 .....
Pattern pass 5 .....
FAILURE INFO:
  RSS1; PP1; RDRAM 2;                RDRAM_ADDR 0x0160218a8;
  X 833 Y 29; EXP 0xa5a5a5a5;        RCV 0xa5aae5ae
                                         -ERROR-

***** Framebuffer RDRAM (Using DMA style 005) Test failed.
ErrCode DMA005 Errors 1
The faulty FRU is GM20
```

A.2.2 GE11 Chip Section Error

The following display reports that a failure occured during the GE11 chip section of the gfx test. The failing FRU is the GM10 graphics board.

```
------   Executing GE0 test setup        ------
 GAMERA found in port 0xc
 GAMERA found in port 0xc
     GE11 Ucode Dnload Test passed.
testing ge0_setup 5....
 GAMERA found in port 0xc
testing getest 1....
 mg_ge_cram in progress
     GE11 cram Test passed.
testing getest 2....
 mg_ge_eram in progress
     GE11 eram Test passed.
testing getest 3....
 mg_ge_wram in progress
     GE11 wram Test passed.
testing getest 4....
 give more delay
testing getest 5....
 mg_ge_alu in progress

*************GE11 Alu Test Failed     -Error-

*************GE11 alu test failed.      ErrCode GEE008  Errors 1
The faulty FRU is GM10

Failure detected in 1GE test
Failure detected in graphics.
```

A.3 Sample Output after an Unexpected Exception

When an unexpected exception occurs, Octane_ide displays a dump of the contents of the CPU and heart registers. If this exception occurs, you must either reset the system or press the Enter key to return to the System Maintenance menu.

In the following example, an exception occurred when the Shoebox test was initiated on a system that was not configured with a PCI Shoebox.

```
ide>> shoebox

Starting SHOEBOX Tests **********
Running All PCI Shoe Box Tests
Testing Bridge at xbow port 0xd, addr 0x900000001d000000

Exception: <vector=Normal>
Status register: 0x24000082<CU1,FR,IPL=8,KX,MODE=KERNEL>
Cause register: 0xc01c<CE=0,IP8,IP7,EXC=DBE>
Exception PC: 0xa8000000208692e8, Exception RA: 0xa8000000208692c0
Data Bus error
HEART ISR :      0x8004000000000000<HEART_EXC,TIMER>
HEART IMSR:      0x8000000000000000<HEART_EXC>
     Cause: 0x10000<WIDGET_ERR>
        Widget Error type: 0x8<PIO_RD_TIMEOUT>
        PIO rd timeout address:
0xd000<CPU=0,IO_SPACE=0x0,DIDN=0xd,ADDR=0x0>
  VID 0's saved user regs in hex (gpda=0xa800000020b3c668):
  arg: 900000001d00002c 2c a800000020bd3cd8 1
       0 0 0 0
  tmp: 0 2 2 a800000020a57ac8
  sve: a800000020a6c3d0 a800000020a6c450 10000000 9000000000000000
       a800000020a289e8 a800000020a965c0 a800000020bd3d10 6
  t8 20a289e8 t9 ffffffffcccccccc at 20a70000
  v0 1 v1 0 k1 ffffffffbad11bad
  gp a8000000203c8108 fp 1 sp a800000020bd3d10 ra a8000000208692c0

PANIC: Unexpected exception

[Press reset or ENTER to restart.]
```