SGI HSTL Specification

High Speed Transceiver Logic (HSTL) is a JEDEC specification for electrical interface. SGI has developed a specification that is tailored to its needs and it has been designed so it is more stringent than the JEDEC standards. HSTL interfaces designed to the SGI specification will meet and exceed the JEDEC standards.

1 SCOPE

This standard defines the input and output design specification and test conditions for devices that are designed to operate in the HSTL logic switching range, nominally 0.0V to 1.5V. The standard may be applied to IC's operating on any VDD supply voltage as long as the output drivers do not drive beyond VOH(max) shown in this standard. In most cases the use of a separate output supply voltage source (VDDQ) is expected, though other implementations that meet the parametric requirements of this standard are allowed.

Single ended and differential input buffer specifications as well as various push-pull output driver specifications are incorporated in this standard. The standard is intended to provide for interchangeability between all types of HSTL compliant digital IC's.

2 Standard Structure

The standard is defined in three sections. The first section defines pertinent supply voltage requirements common to all compliant IC's. The second & third sections defines the DC input and output design criteria. The fourth section defines the AC test criteria.

A given IC need not be equipped with the ability to support all three classes of output buffer, but each must support at least one HSTL class in order to claim output compliance. The full input reference level (VREF) range specified is required on each IC in order to allow any HSTL IC to receive signals from any HSTL output buffer.

3 Supply Voltage

3.1 DC Supply Voltage Levels

TABLE 1. DC Supply Voltage Levels

Symbol	Parameter	Min	Nom	Max	Units	Notes
VDD	Device Supply Voltage	3.0		3.6	V	
VDDQ	Output Supply Voltage	1.4	1.5	1.6	V	1
VREF	Input Reference Levels	0.6	0.95	1.3	V	1

Notes:

1. The values specified in the table are DC design criteria only.

4 HSTL Input Receivers

4.1 DC Single Ended Input Thresholds

TABLE 2. DC Single Ended Input Logic Levels

Symbol	Parameter	Min	Nom	Max	Units	Notes
VIHT	DC Input Logic Threshold High			VREF + 50mV	V	1,2
VILT	DC Input Logic Threshold Low	VREF - 50mV			V	1,2
VIH	DC Input Voltage High			VDDQ + 0.6	V	
VIL	DC Input Voltage Low	-0.3			V	

Notes:

1. These are DC design criteria only.

2. Output levels from the differential receiver should be at valid output voltage levels for the specified input voltages.

4.2 DC Differential Input Thresholds

TABLE 3. DC Differential Input Logic Levels

Symbol	Parameter	Min	Nom	Max	Units	Notes
VDIF	Differential Input Voltage	0.1		VDDQ + 0.6V	V	1
VCM	Common Mode Input Range	0.65		1.25	V	2
VIH	DC Input Voltage High			VDDQ + 0.3	V	
VIL	DC Input Voltage Low	-0.3			V	

Notes:

1. VDIF specifies the minimum input differential voltage (VTR - VCP) required for switching, where VTR is the “true” input level and VCP is the “complement” input level.

2. VCM specifies the allowable input range for which the receiver must receive valid data. Min = VREF(min) + VDIF(min)/2 & Max = VREF(max) - VDIF(min)/2

5 HSTL Output Drivers

HSTL output devices are specified as one of three classes. The following are the DC design criteria for these devices.

5.1 Type Ia: Push-Pull Output Buffer for Unterminated Loads

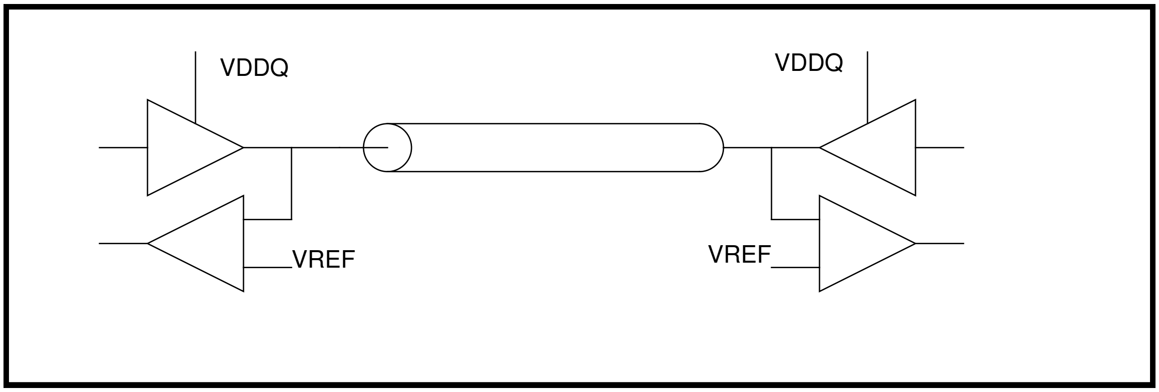
TABLE 4. DC Design for Output Driver Logic Levels

Symbol	Parameter	Min	Nom	Max	Units	Notes
VOH	DC Output Logic High	VDDQ			V	1
VOL	DC Output Logic Low			0.0	V	1

Notes:

1. These values are DC only

FIGURE 1. HSTL Unterminated



5.2 Type Ib: Push-Pull Output Buffer Internally Series Terminated

Type Ib output buffers differ only from Type Ia in that they have a series output resistor.

TABLE 5. DC Design for Output Driver Logic Levels

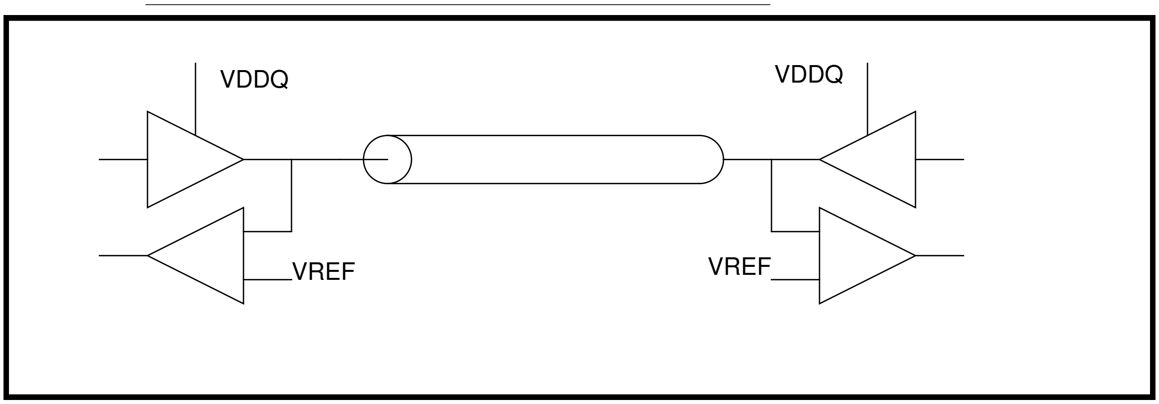
Symbol	Parameter	Min	Nom	Max	Units	Notes
VOH	DC Output Logic High	VDDQ			V	1
VOL	DC Output Logic Low			0.0	V	1
RS	DC Series Output Resistance		15		Ω	2

Notes:

1. These values are DC only

2. The series resistance is defined as fully turn-on or off resistance.

FIGURE 2. HSTL Internally Series Terminated



5.3 Type IIa: Push-Pull Output Buffer for Symmetrically Terminated Load

TABLE 6. DC Design for Output Driver Logic Levels

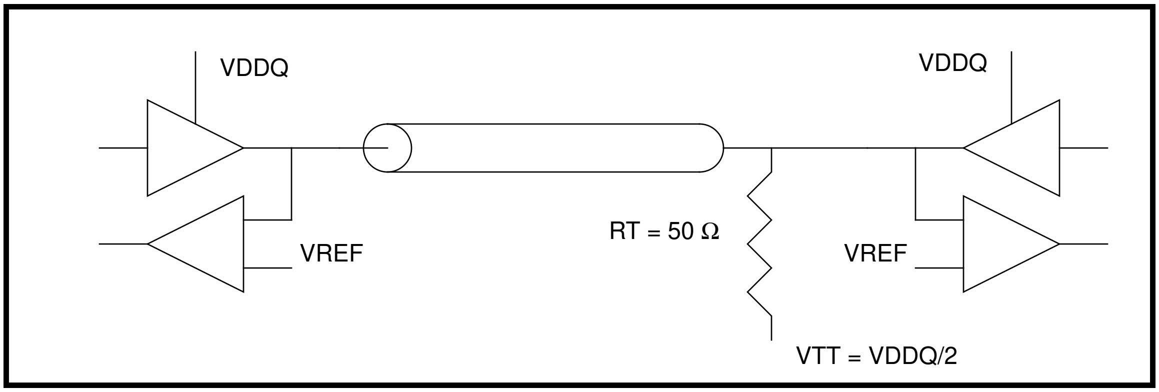
Symbol	Parameter	Min	Nom	Max	Units	Notes
VOH	DC Output Logic High	VDDQ - 0.2			V	1
VOL	DC Output Logic Low			0.2	V	1

Notes:

1. These are DC values only.

For the symmetrically terminated lines VTT must not be equal to VREF. | VTT - VREF | > 100mV.

FIGURE 3. HSTL Symmetrically Terminated Load



5.4 Type IIb: Push-Pull Output Buffer for Symmetrically Parallel Terminated Load

TABLE 7. DC Design for Output Driver Logic Levels

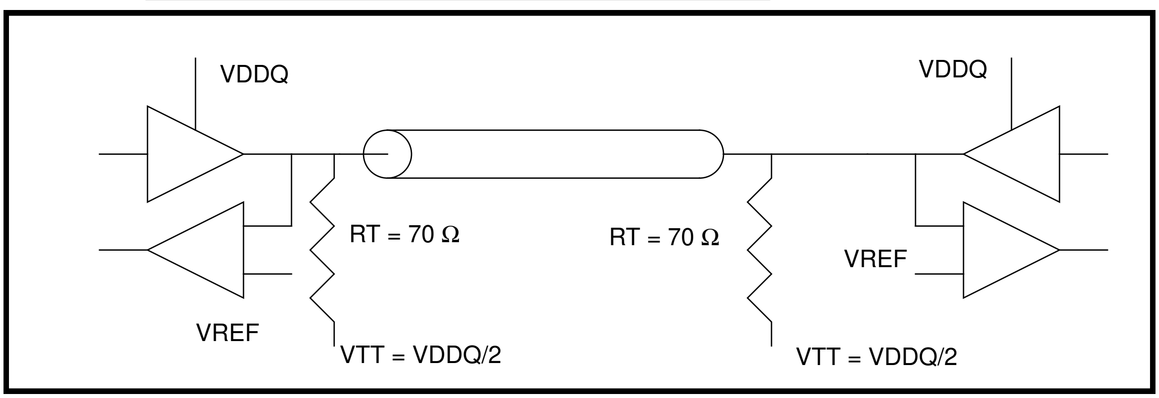
Symbol	Parameter	Min	Nom	Max	Units	Notes
VOH	DC Output Logic High	VDDQ - 0.3			V	1
VOL	DC Output Logic Low			0.3	V	1

Notes:

1. These are DC values only.

For the symmetrically terminated lines VTT must not be equal to VREF. | VTT - VREF | > 100mV.

FIGURE 4. HSTL Symmetrically Parallel Terminated Load



5.5 Type IIIa: Push-Pull Output Buffer for Asymmetric Terminated Load

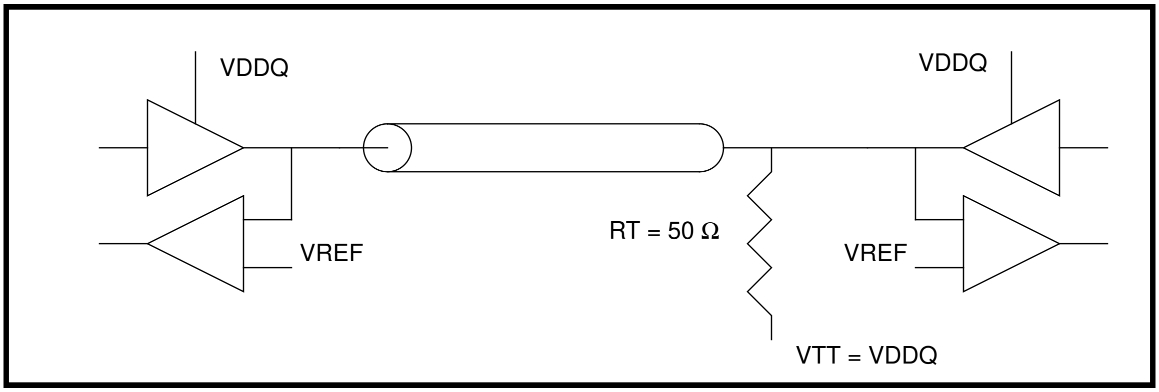
TABLE 8. DC Design for Output Driver Logic Levels

Symbol	Parameter	Min	Nom	Max	Units	Notes
VOH	DC Output Logic High	VDDQ			V	1
VOL	DC Output Logic Low			0.4	V	1

Notes:

1. These are DC values only

FIGURE 5. HSTL Asymmetrically Terminated



5.6 Type IIIb: Push-Pull Output Buffer for Asymmetric Parallel Terminated Load

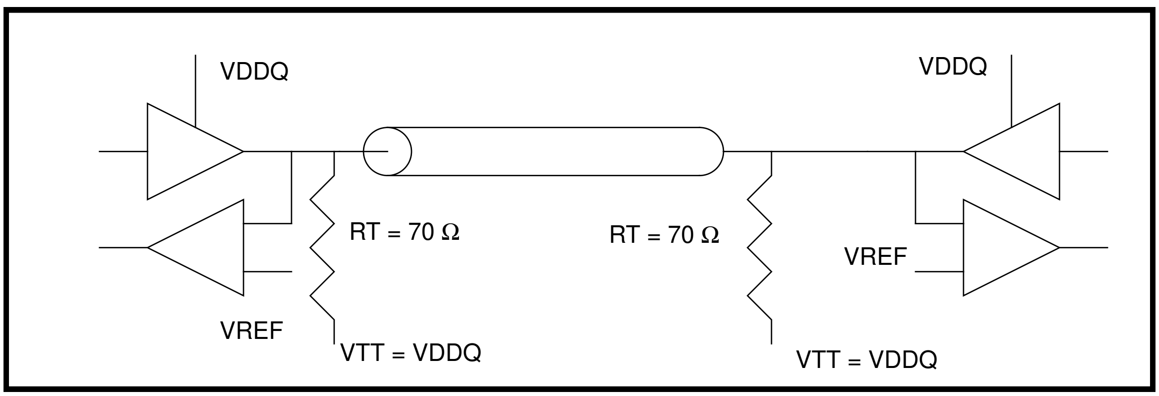
TABLE 9. DC Design for Output Driver Logic Levels

Symbol	Parameter	Min	Nom	Max	Units	Notes
VOH	DC Output Logic High	VDDQ			V	1
VOL	DC Output Logic Low			0.55	V	1

Notes:

1. These are DC values only.

FIGURE 6. HSTL Asymmetrically Parallel Terminated



6 AC Design Criteria

The AC design criteria defines the operating frequency of the input receivers and output drivers. This part of the specification is defined for high frequency operation.

TABLE 10. AC Design Criteria

Symbol	Parameter	Min	Nom	Max	Units	Notes
F	Operating frequency			200	MHz	1
TSLEW	Output Rise/Fall Time			400	ps	2

TABLE 10. AC Design Criteria

Symbol	Parameter	Min	Nom	Max	Units	Notes
VIH	DC Input Voltage High	Vref + 0.3			V	3
VIL	DC Input Voltage Low			Vref - 0.3	V	3

Notes:

1. At this operating frequency all inputs and outputs specified are guaranteed to operate and meet all DC voltage specifications for valid logic transitions.

2. TSLEW is characterized into the package of interest with an ideal 50 ohm transmision line load that is ideally terminated.

3. VIH & VIL are the guaranteed minimum input swing to the differential receiver for which must be guaranteed to operate at for the given F.