R10000 Superscalar Microprocessor

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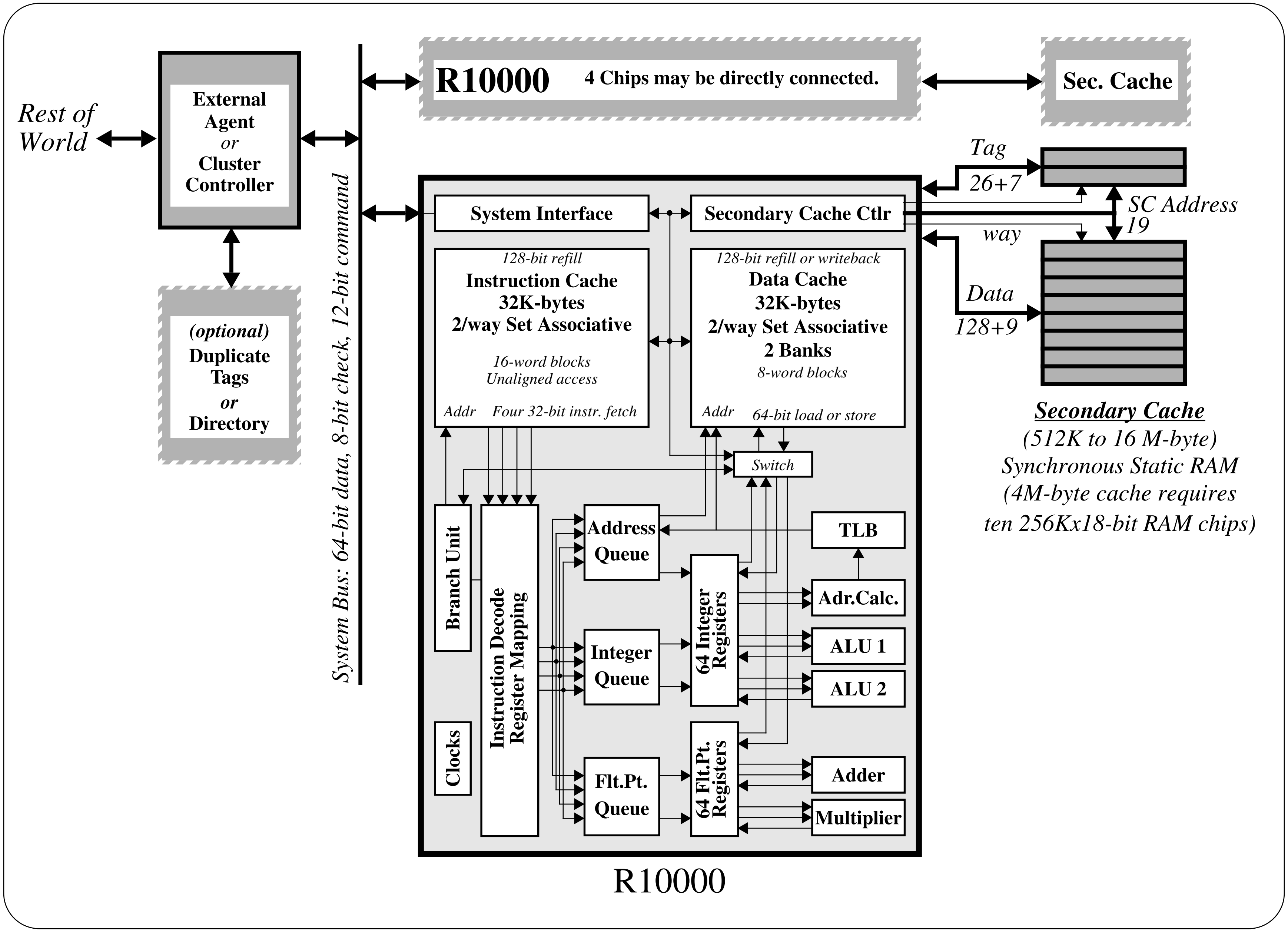
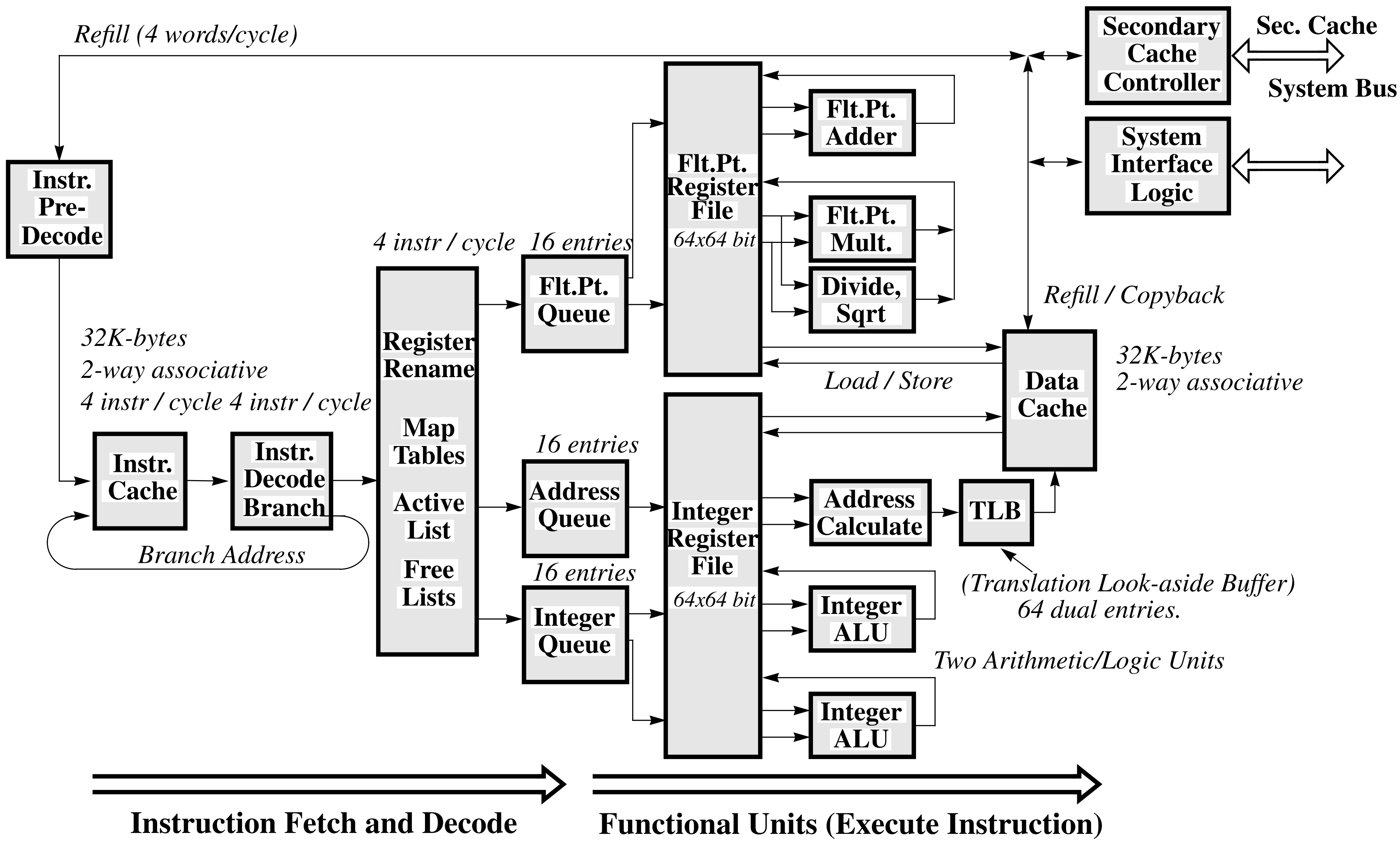
Presentation Outline

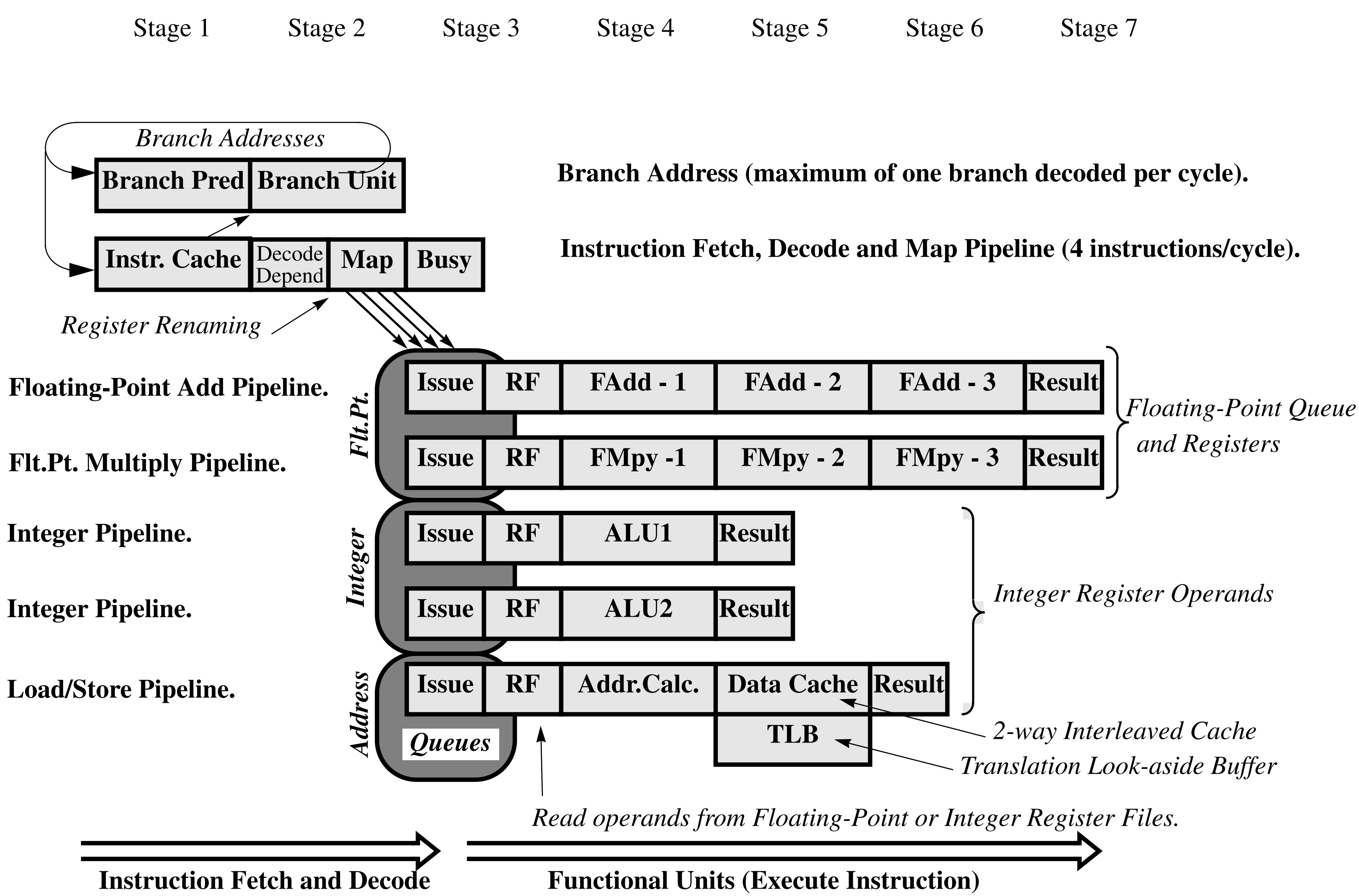
- Architecture of CPU and FPU
- Memory Hierarchy
- System Configuration
- Verification and Design Methods


Rest of World
External Agent or Cluster Controller
(optional) Duplicate Tags or Directory
System Bus: 64-bit data, 8-bit check, 12-bit command
R10000
4 Chips may be directly connected.
Sec. Cache
Tag
26+7
SC Address
19
way
Data
128+9
System Interface
Secondary Cache Ctlr
128-bit refill
Instruction Cache
32K-bytes
2/way Set Associative
16-word blocks
Unaligned access
Addr
Four 32-bit instr. fetch
128-bit refill or writeback
Data Cache
32K-bytes
2/way Set Associative
2 Banks
8-word blocks
Addr
64-bit load or store
Switch
Branch Unit
Instruction Decode
Register Mapping
Clocks
Address Queue
Integer Queue
Flt.Pt. Queue
64 Integer Registers
64 Flt.Pt. Registers
TLB
Adr.Calc.
ALU 1
ALU 2
Adder
Multiplier
Secondary Cache
(512K to 16 M-byte)
Synchronous Static RAM
(4M-byte cache requires
ten 256Kx18-bit RAM chips)
R10000

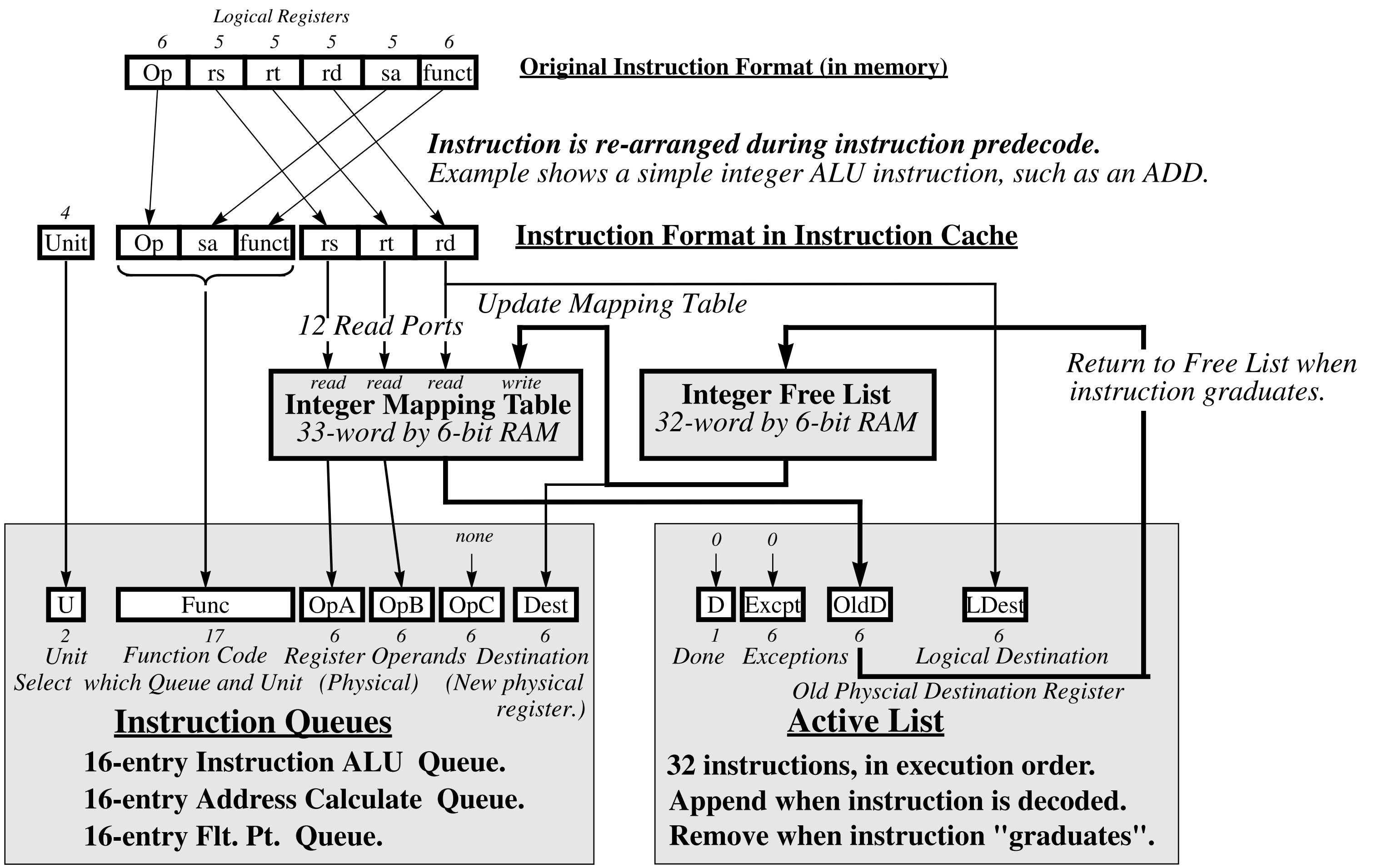
R10000 - Block Diagram



R10000 - Pipelines

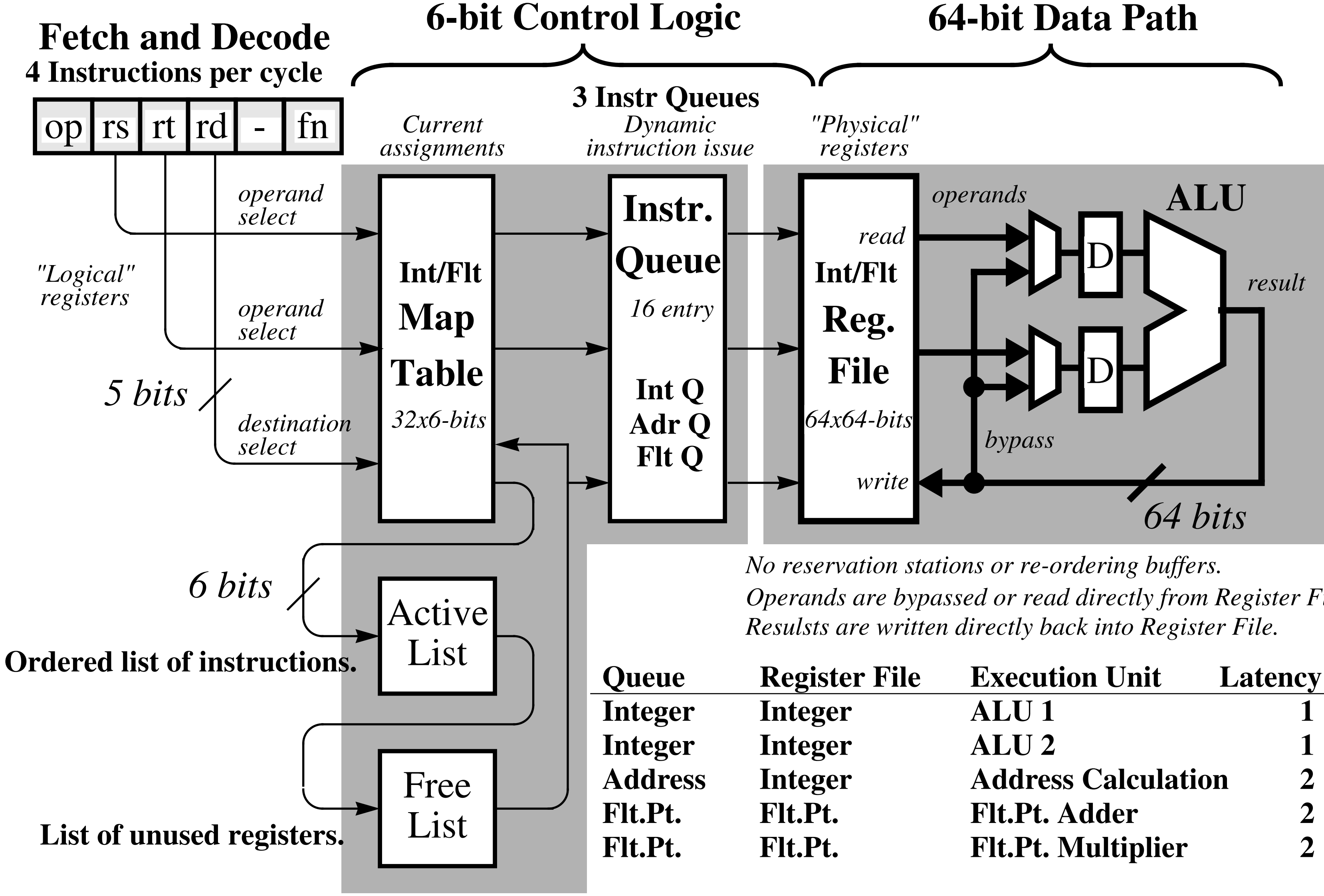


Register Renaming



During any cycle, each physical register number is either in Mapping Table, Active List, or Free List.

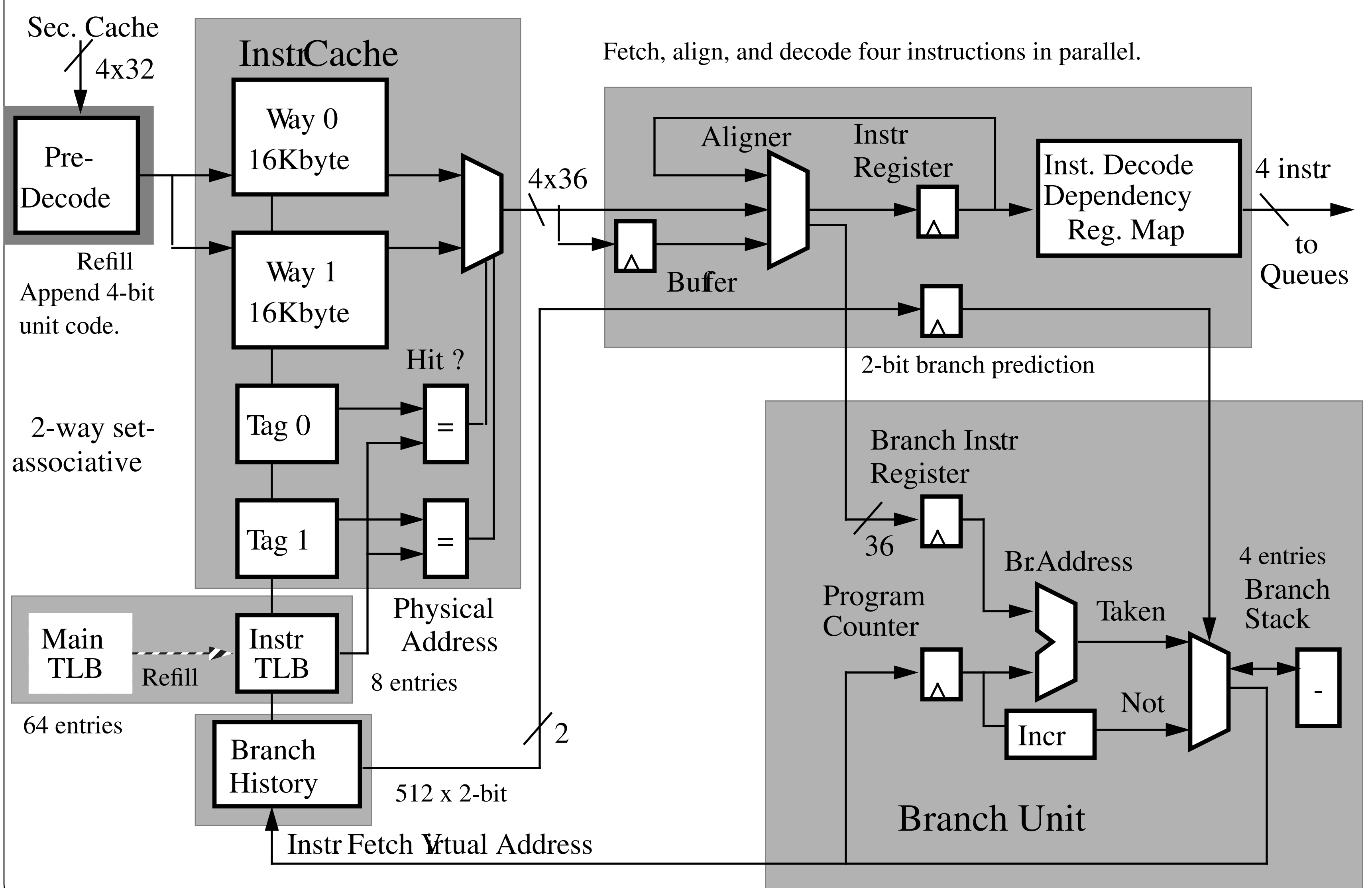
Control Paths



No reservation stations or re-ordering buffers.
Operands are bypassed or read directly from Register File.
Resulsts are written directly back into Register File.

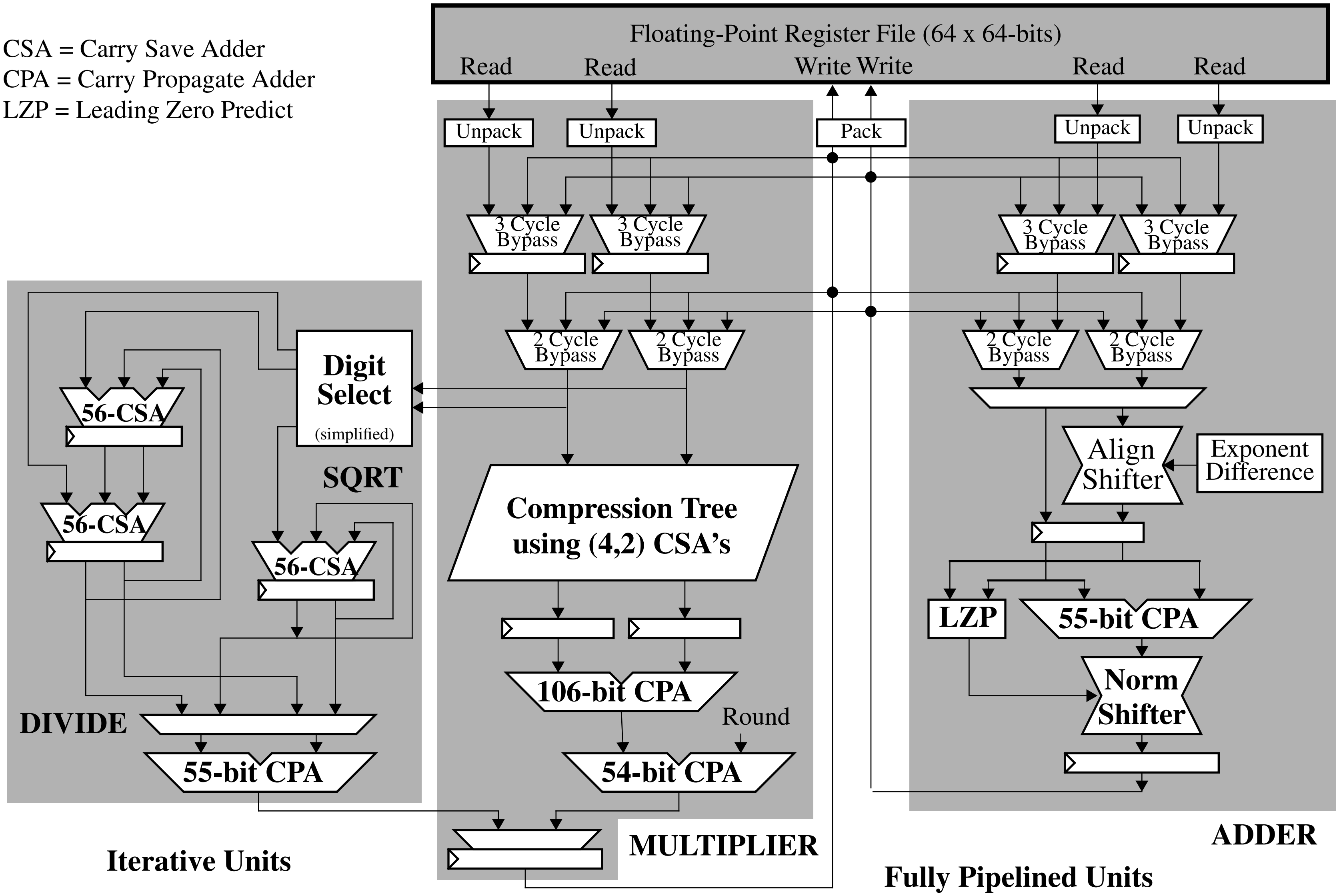
Queue	Register File	Execution Unit	Latency
Integer	Integer	ALU 1	1
Integer	Integer	ALU 2	1
Address	Integer	Address Calculation	2
Flt.Pt.	Flt.Pt.	Flt.Pt. Adder	2
Flt.Pt.	Flt.Pt.	Flt.Pt. Multiplier	2

Instruction Fetch and Branch

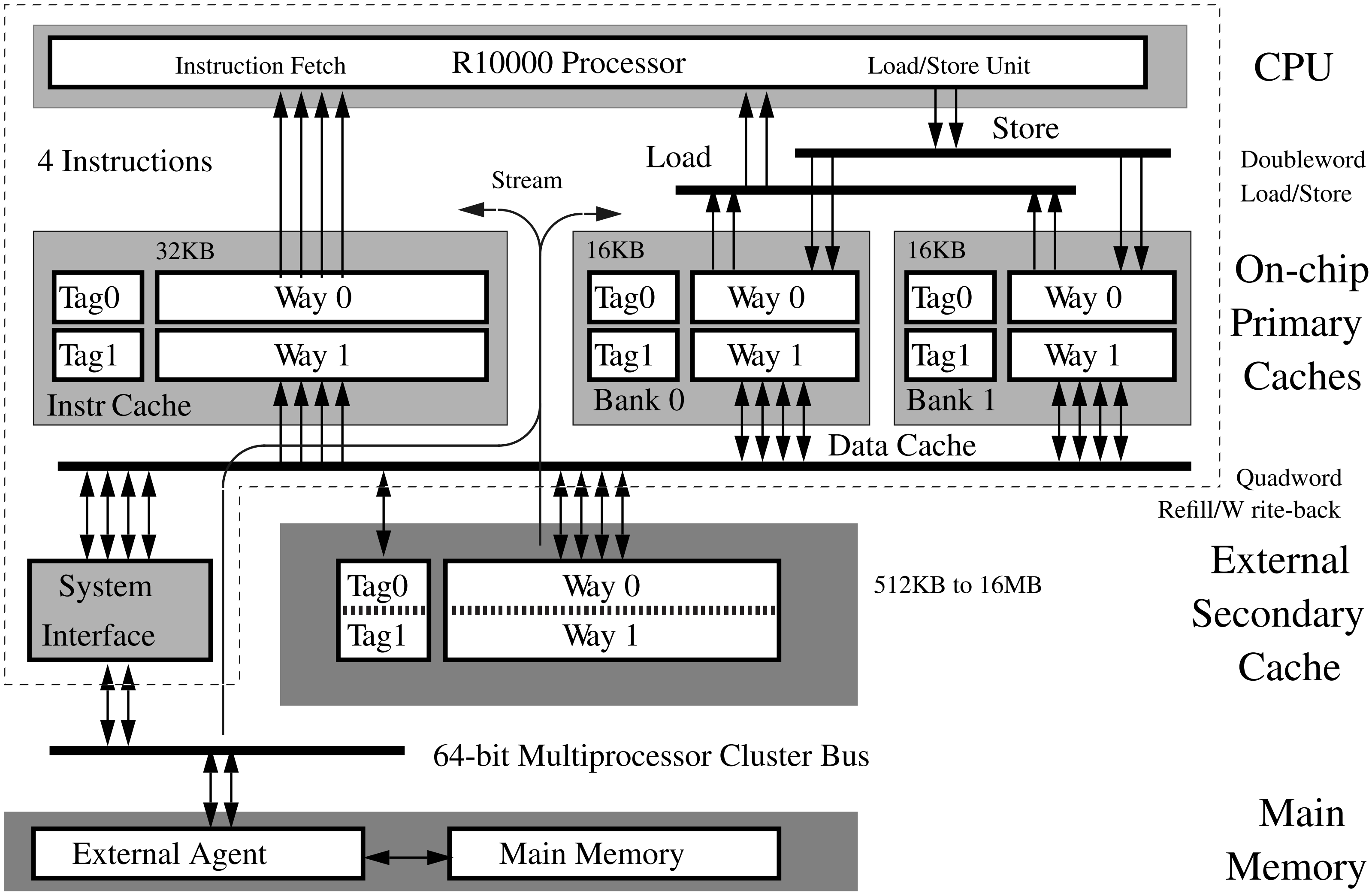


Floating-Point Units

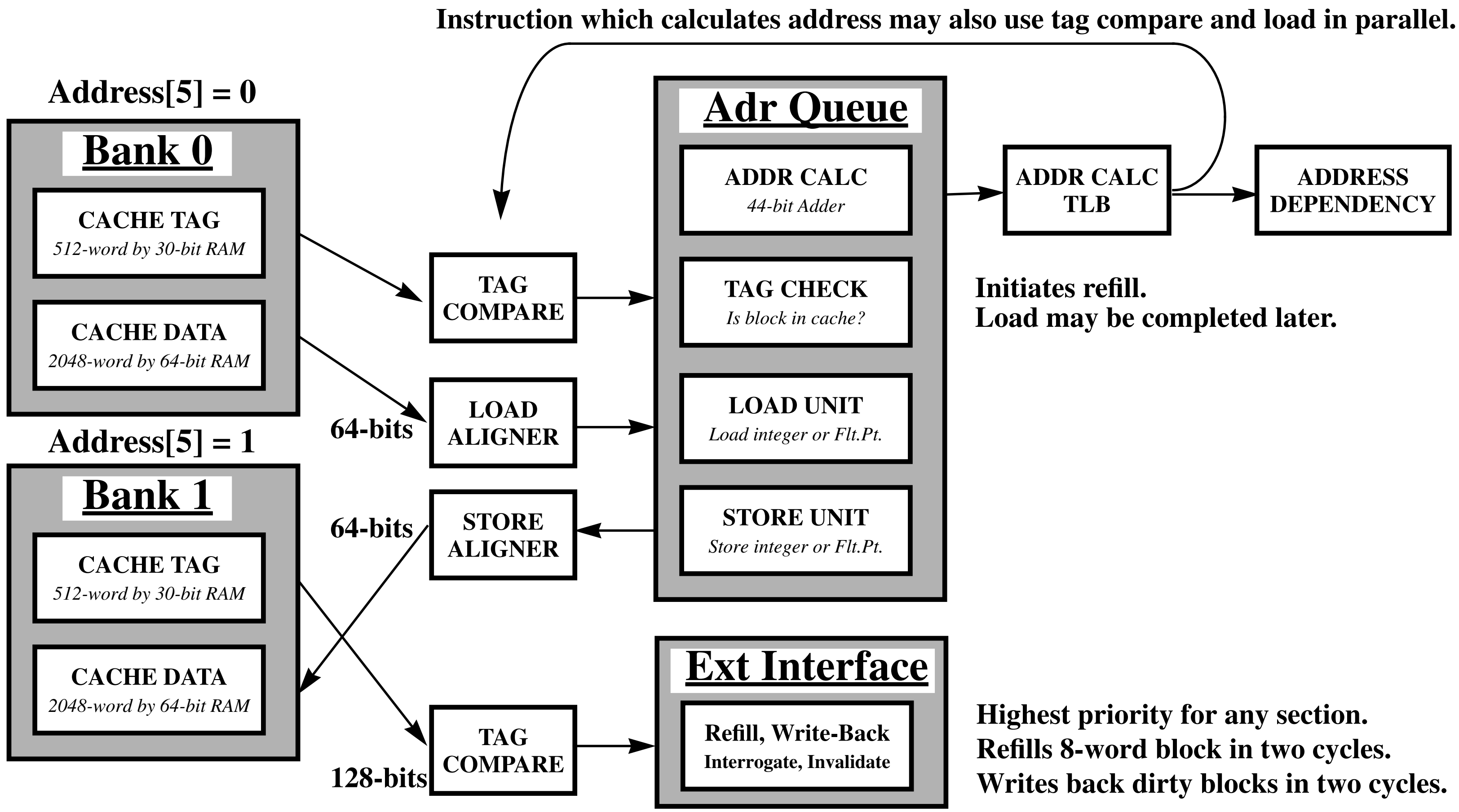
CSA = Carry Save Adder
CPA = Carry Propagate Adder
LZP = Leading Zero Predict



R10000 Memory Hierarchy



Parallelism in Data Cache



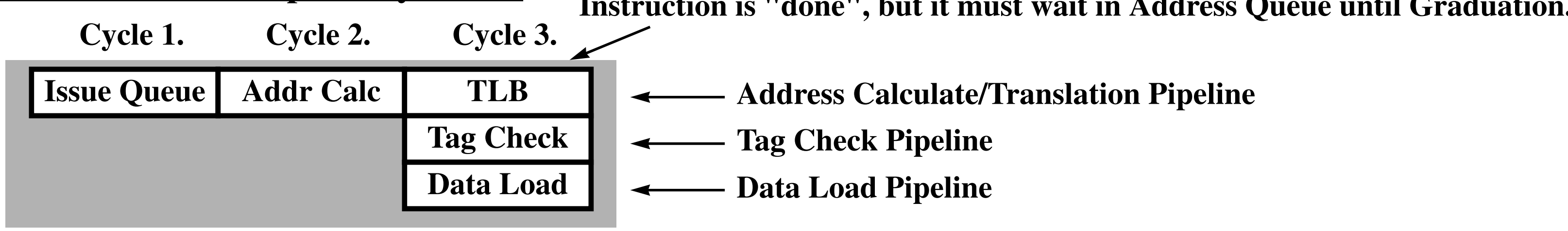
<u>Four sections can be independently allocated.</u>

<u>Five control units can operate in parallel, if resources do not collide.</u>

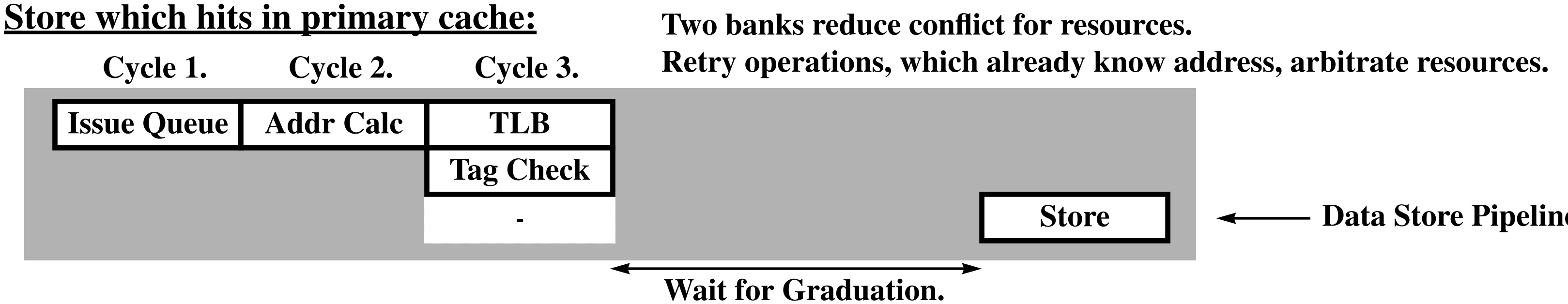
CPU accesses are 64 bits wide, 2-way associative.
Refill and write-back are 128 bits wide. (Way is known.)

Data Cache Pipelines

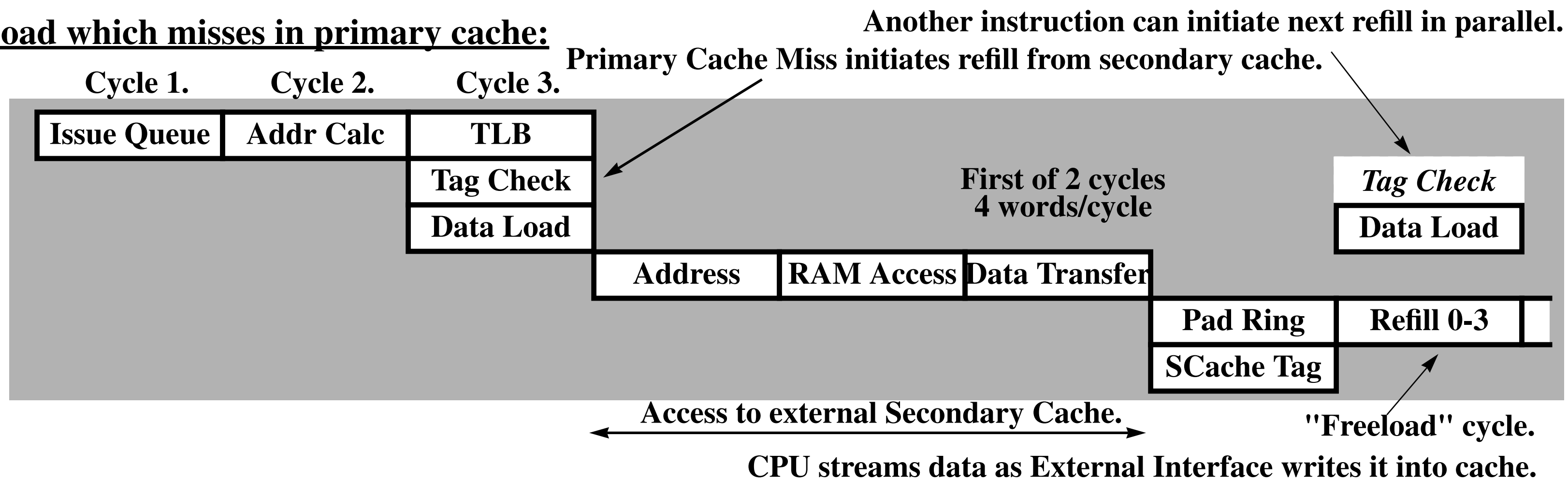
Load which hits in primary cache:



Store which hits in primary cache:

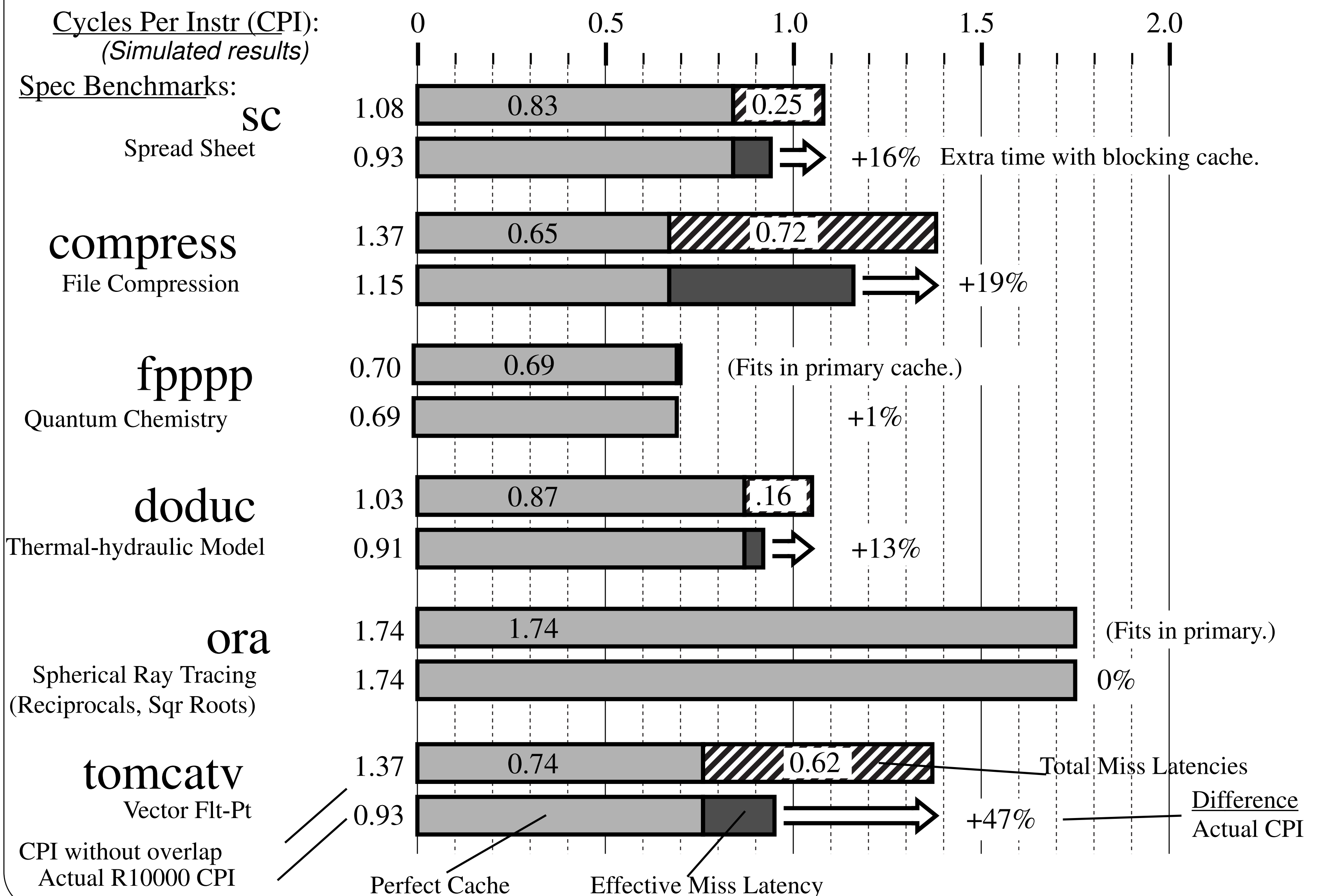


Load which misses in primary cache:

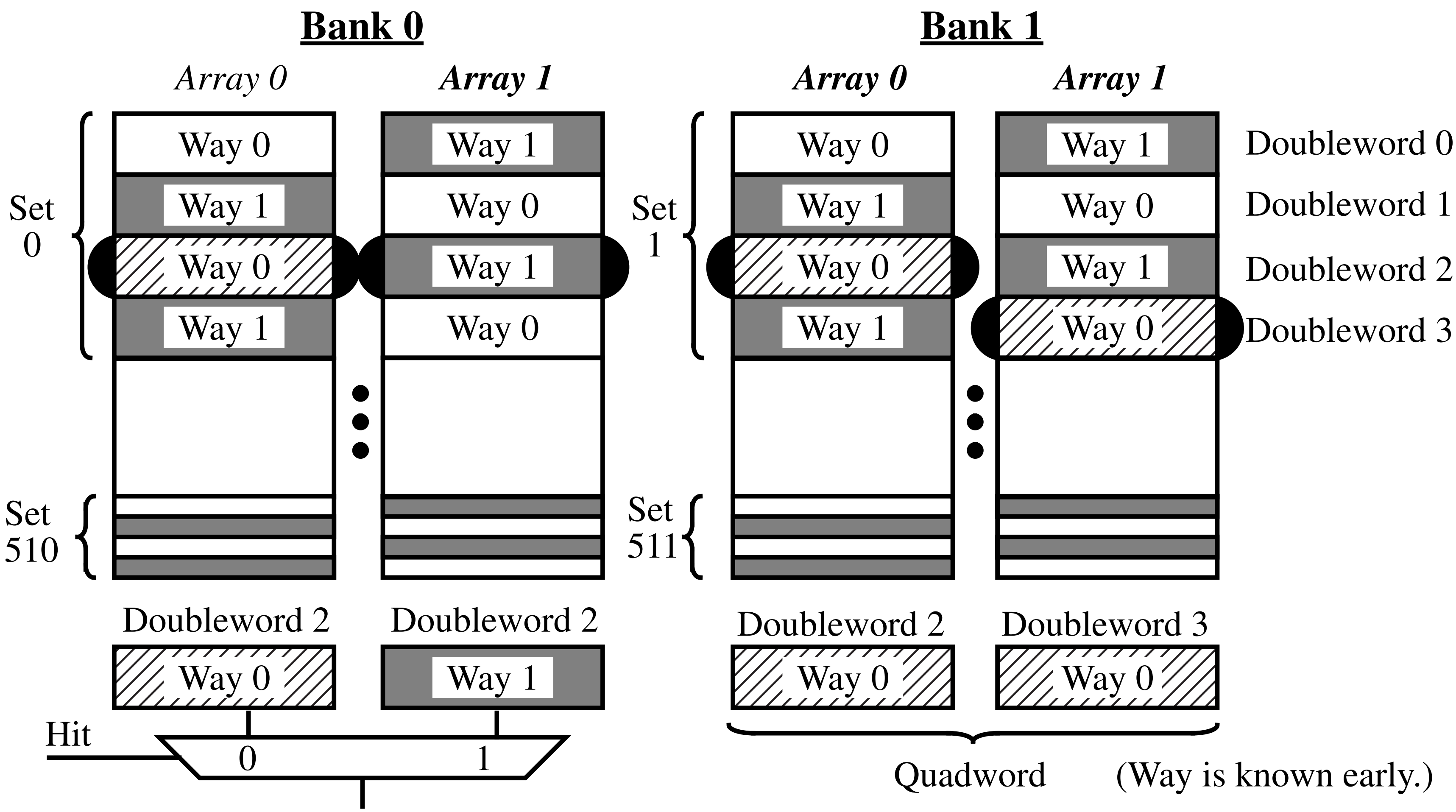


Non-blocking Cache

Concurrent refill times reduce effective cache latency.



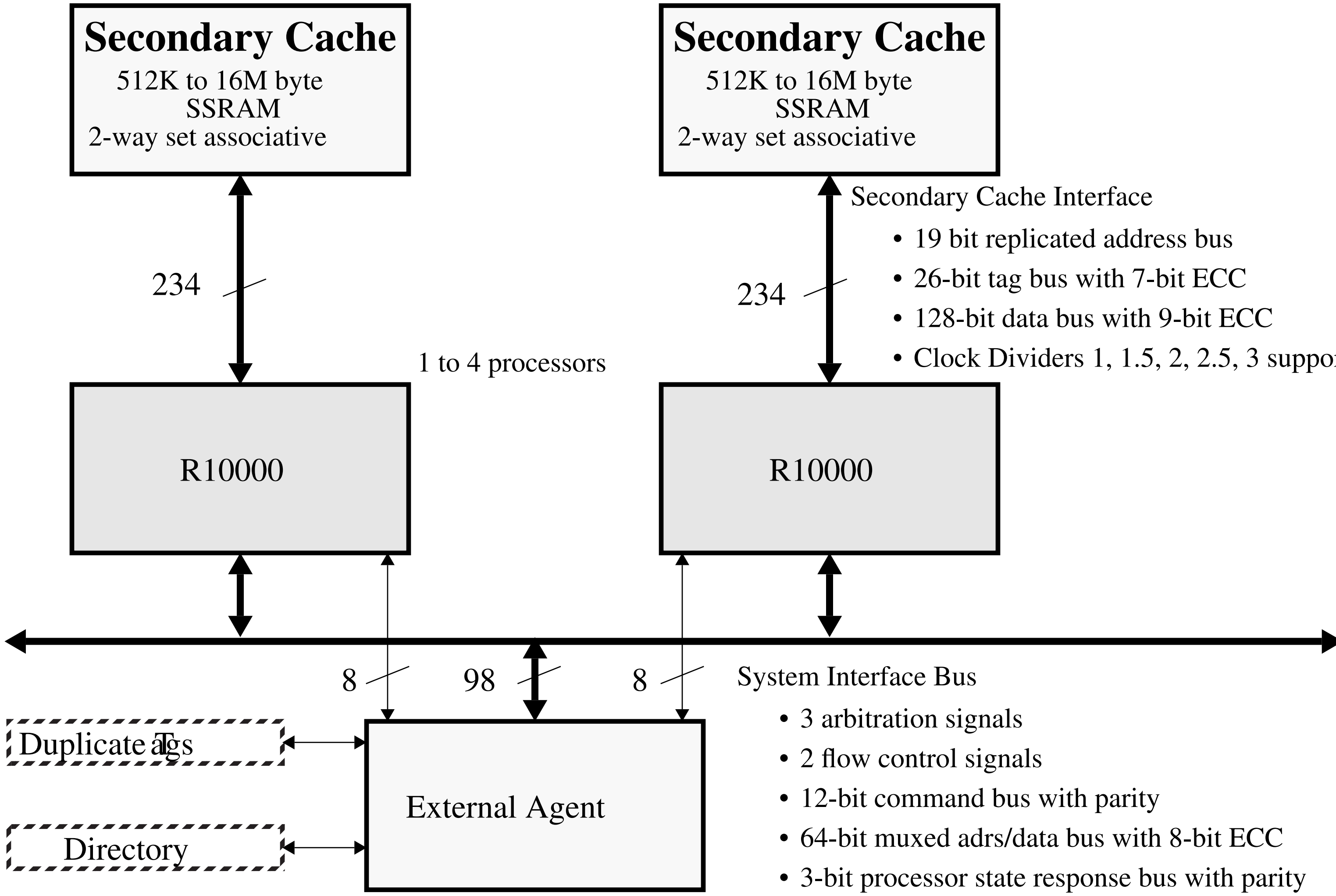
Data Cache Interleaving



CPU accesses one doubleword.
Simultaneous tag check selects way.

External Interface accesses quadword
as two doublewords in parallel.

System Configurations



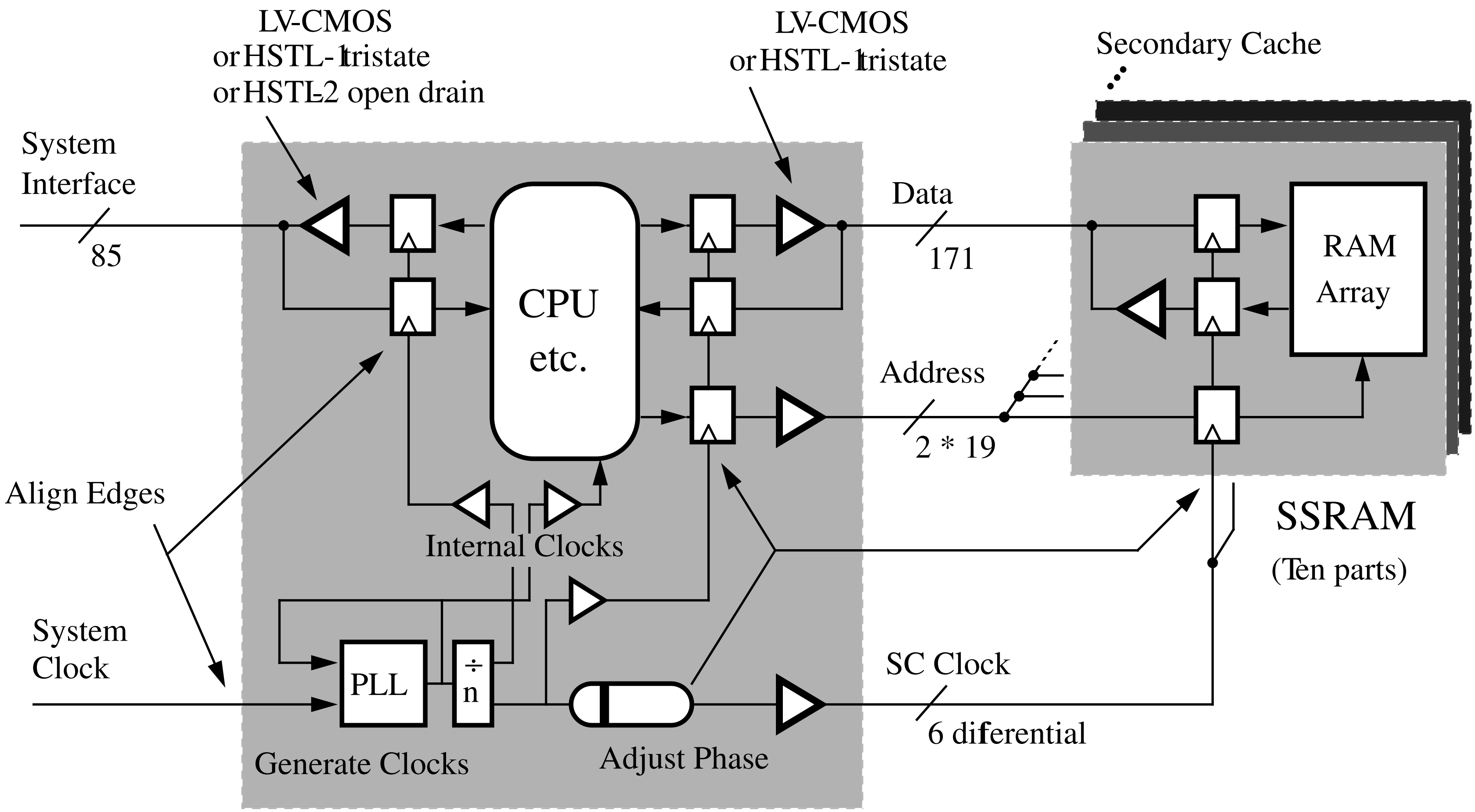
Secondary Cache Interface

- 19 bit replicated address bus
- 26-bit tag bus with 7-bit ECC
- 128-bit data bus with 9-bit ECC
- Clock Dividers 1, 1.5, 2, 2.5, 3 supported

System Interface Bus

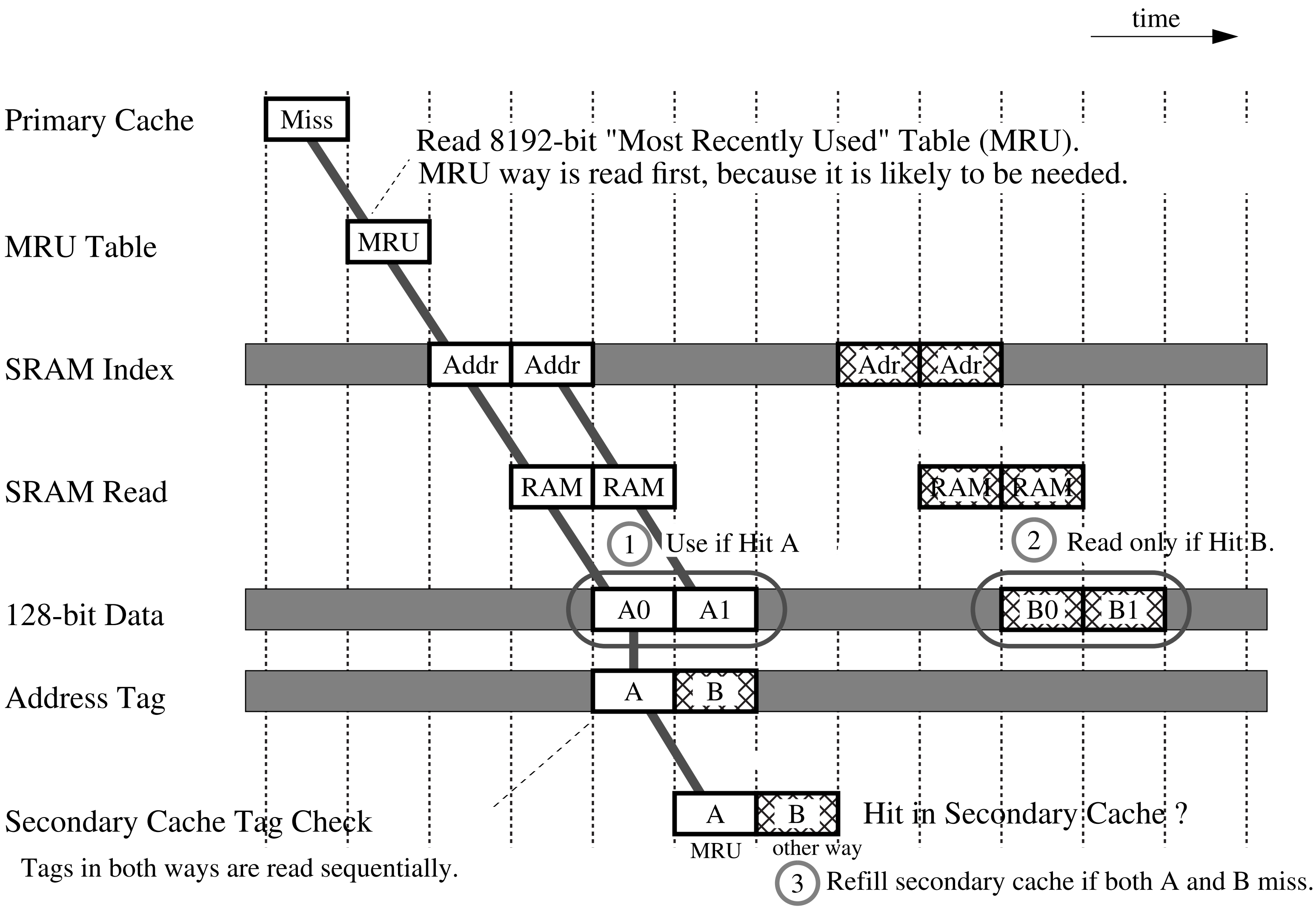
- 3 arbitration signals
- 2 flow control signals
- 12-bit command bus with parity
- 64-bit muxed adrs/data bus with 8-bit ECC
- 3-bit processor state response bus with parity
- 5-bit external response bus with parity
- Clock Dividers 1, 1.5, 2, 2.5, 3, 3.5, 4 supported

Clocks and Output Drivers

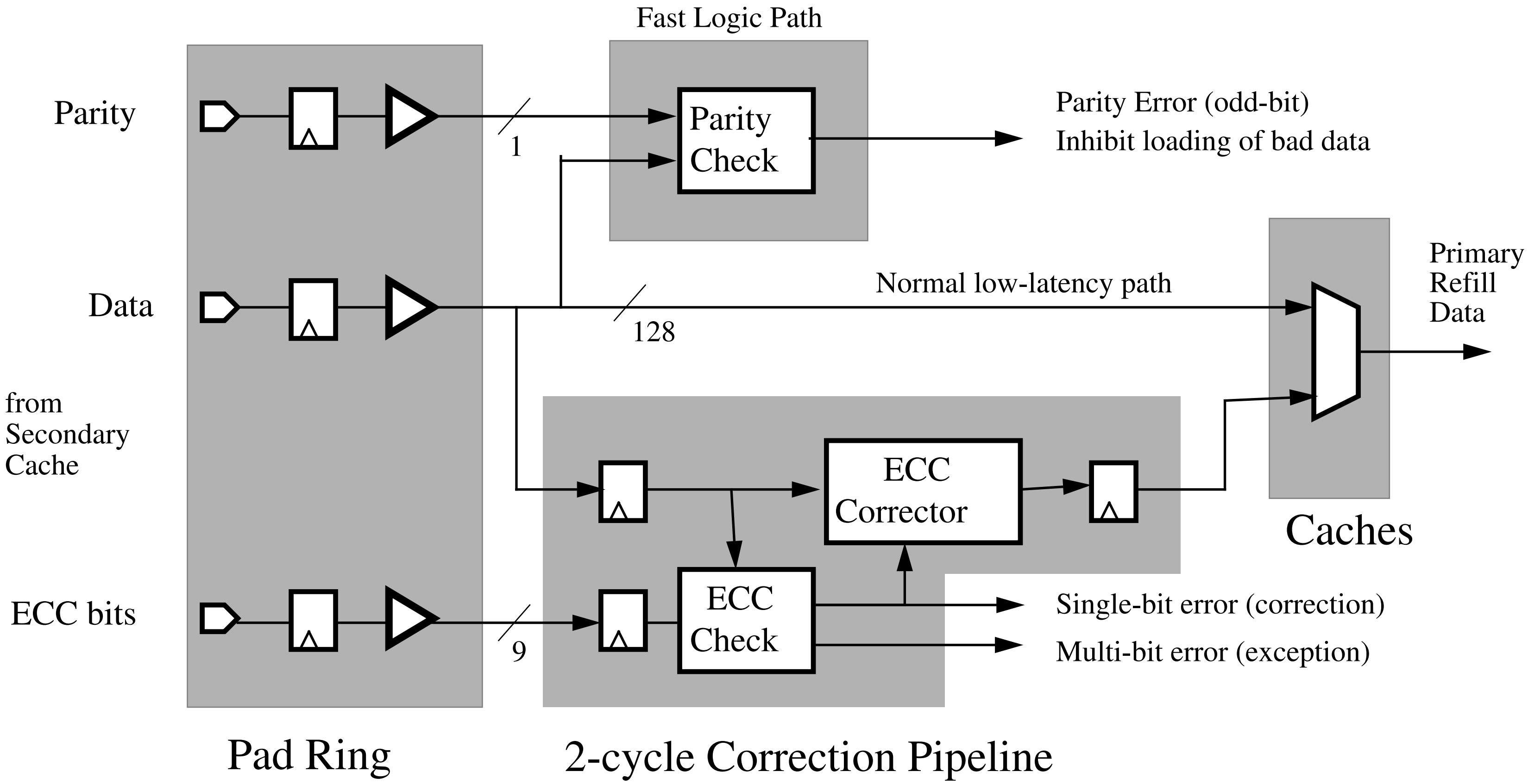


R10000 Microprocessor

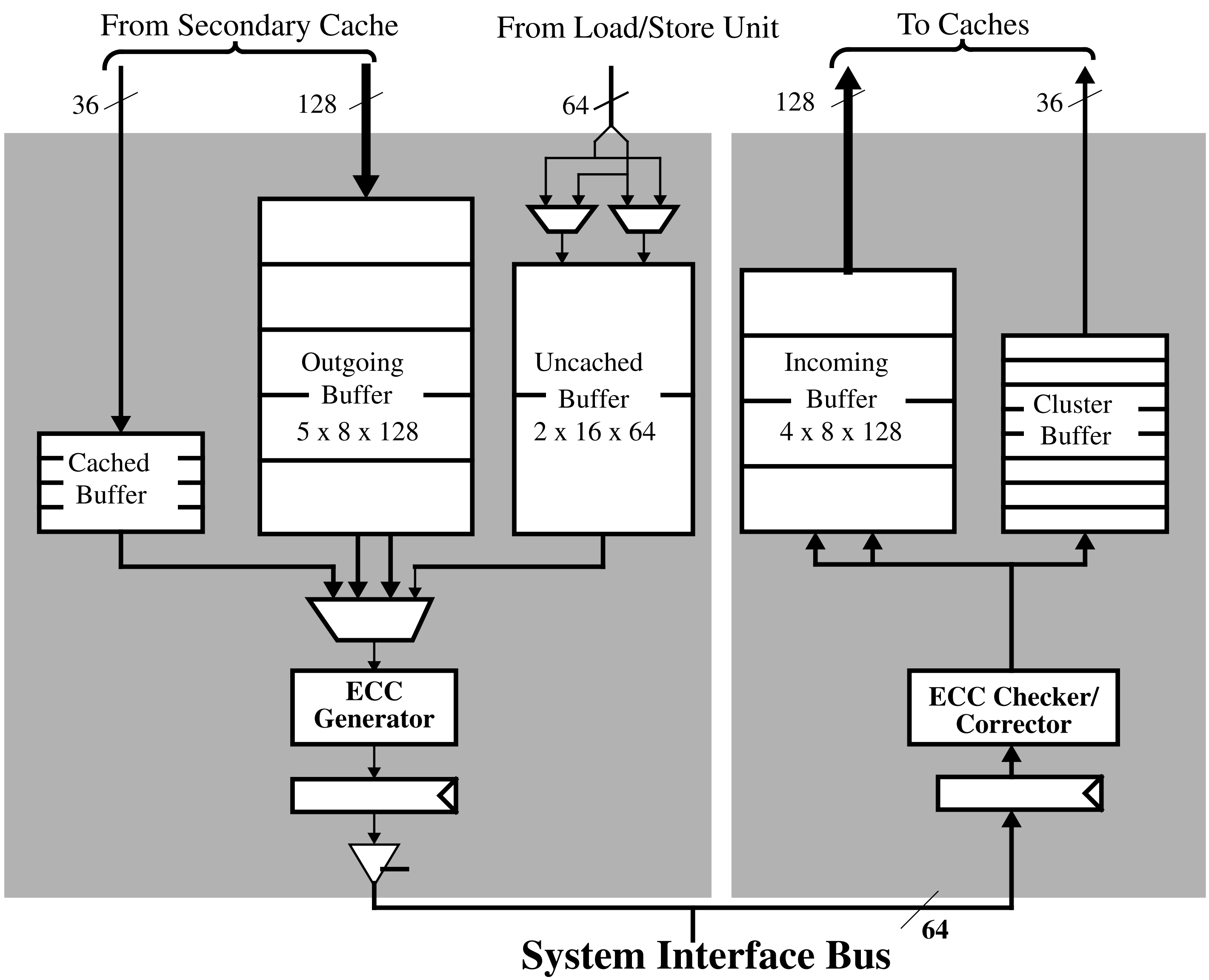
Refill from Set-Associative Secondary Cache



Secondary Cache Error Protection



System Interface Block Diagram



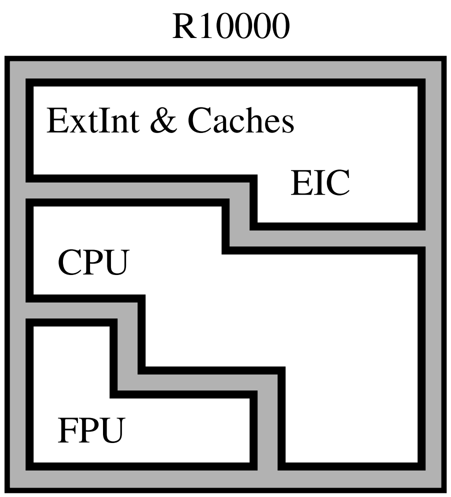
Functional Verification Methodology

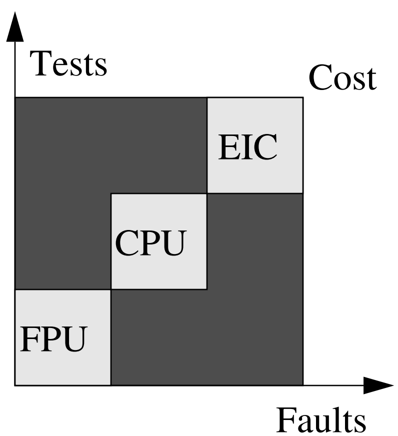
- Tools and environment:
  - Inhouse HDL and simulator with backup and replay.
  - Graphical user interface for simulation and regression.
  - An instruction level simulator as a reference machine, which checks
    - Architecture registers
    - Memory hierarchy
  - Programmable random code generators for UP and MP.
  - Arc coverage and consistency checking for state machines.
- C-based System Model supports
  - Secondary cache array, memory controller and array, bus controller.
  - Bus protocol checking.
  - External events :
    - programmable or purely random
    - imbeded in diagnostics for fine-grain control
  - 1 to 4 processor configuration.

Diagnostic Development

- Directed Diagnostics
  - Architecture Verification Programs (AVP)
  - Microarchitecture Verification Programs (MVP)
  - Implementation Verification Programs (IVP)
- Random Diagnostics From Programmable Random Code Generators
  - Functional unit intensive
  - Load/Store intensive
  - Branch intensive
  - Mix of the above under UP and MP environments
- Diags are self-checking and/or compared with the reference machine.
- UP and MP applications.
- Booting O/S's on R10000 RTL : 2 Unix O/S's and NT.

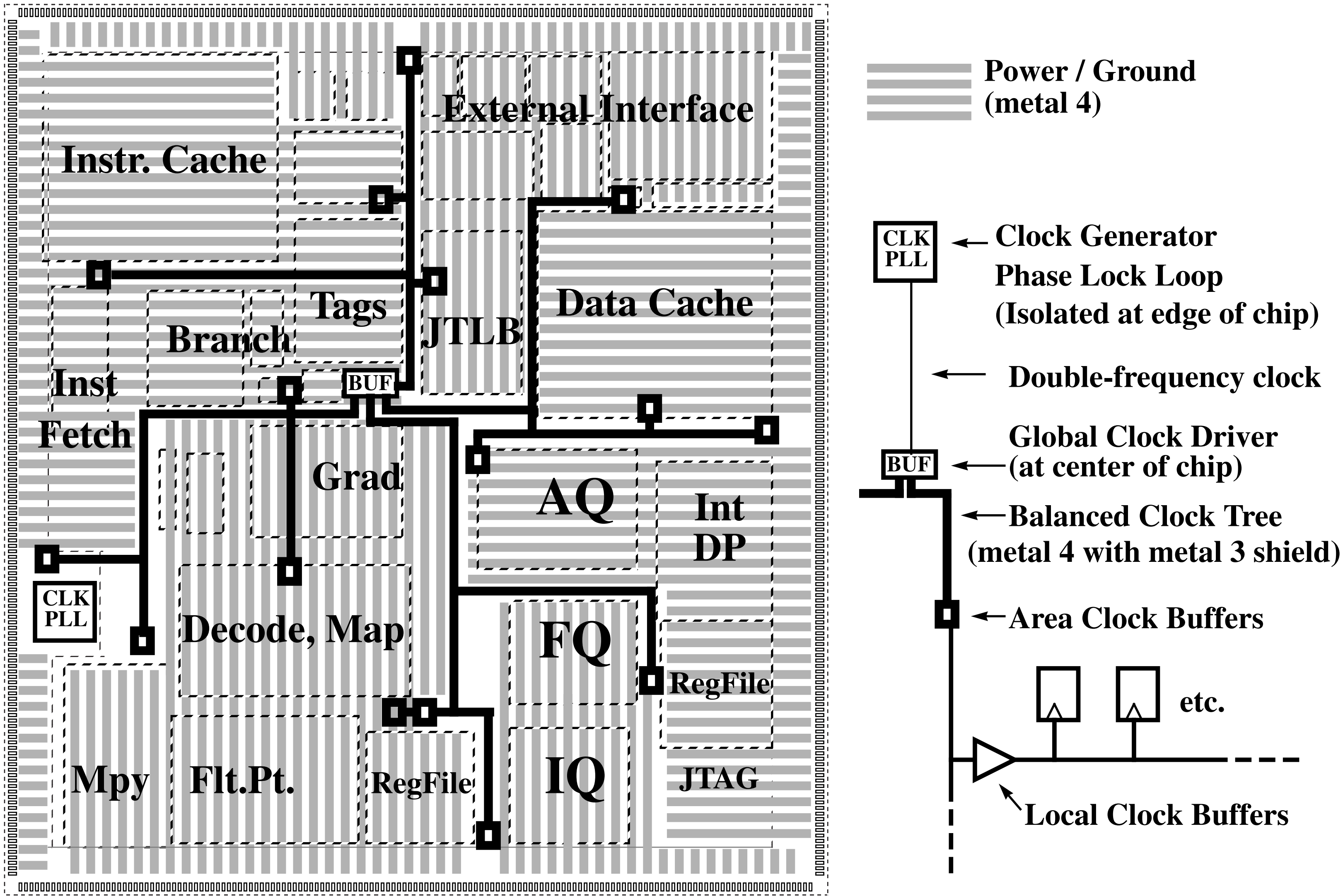
Test Features



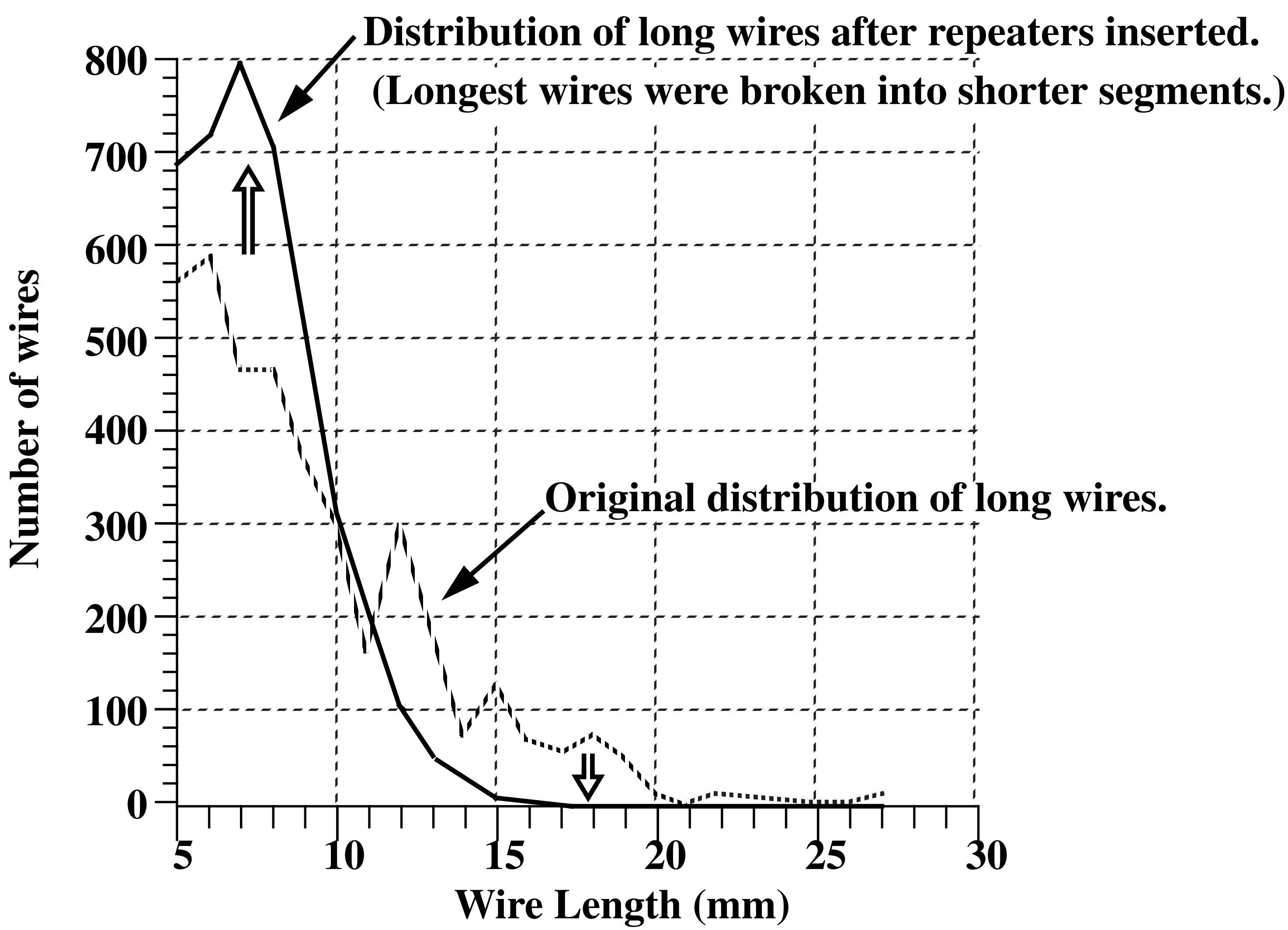


- On-chip virtual output pins:
  - Physical design partitioning
  - Direct observability of internal signals
  - Signature compression through LFSRs
    (Linear-Feedback Shift Register)
- Dedicated test structures:
  - No performance impact
  - No logic design overhead
  - No special clock requirements
- Enhanced debug and diagnostics:
  - Cycle-by-cycle sampling of internal signals
  - Observed signals correlate to logic specification
  - Signature analysis
- Test cost reduction:
  - No special ATE requirements
  - Internal test-output compression by signature
  - Test and fault partitioning.
  - Reduced test time and higher fault coverage

Clock and Power Distribution



Signal Repeaters on Long Wires



R10000 Die Photo

This sheet shows physical placement of major blocks.
(Full color photo slide will be shown at Hot Chips.)