Differences between R10000 and R4400

R10000

Architecture Implementation

Superscaler

Speculative execution (branch prediction)

Speculative memory access

Out of order execution

Out of order cache miss detection

Non blocking Load/Store

ISA

MIPS IV set - Added Prefetch, Conditional Move I/FP, Index Load/Store FP, etc.

LL/SC, Sync definition and Convert Long, Move instructions different from those in R4400

Caches

PI: 32K, 2-Way, 16Wd block

PD: 32K, 2-Way, 8Wd block

S: 512K-16M, 2-Way, SSRAM, 16 & 32 Wd block (no hardware change)

Instructions are 36-bits pre-decoded

Cache Coherency

No Dirty Shared state

No Link Address Register - hardware makes sure the link address is never replaced

R4400

Architecture Implementation

Superpipeline

No speculation

Execution in sequence

Processor stalls due to cache miss

Pipeline stalls if to cache miss

ISA

MIPS III set

Caches

PI: 16K, Direct map, 4 or 8Wd

PD: 16K, Direct map, 4 or 8Wd

S: 128K to 16M, Direct Map, 4 or 8 or 16 or 32Wd.

Instructions are 32-bits (not pre-decoded)

Cache Coherency

Dirty Shared option

Link Address Register needed if linked line is replaced.

Differences between R10000 and R4400

R10000	R4400
CEx line is owned by memory	CEx line is owned by the processor.
Cache Algorithm	***Cache Algorithm***
No update protocol	Update protocol option
Added uncached accelerated	No uncached accelerated
CP0 & Memory Management	***CP0 & Memory Management***
TLB has 64 entries	TLB has 48 entries
VPN of 44 bits	VPN 40 bits
PFN of 40 bits	PFN of 36 bits without any restriction in any mode.
Phys. Addr. space is limited to 2^{38} if TLB is written in the 32-bit User or Supr. mode.	
Prevents same multiple entry in TLB.	Causes TLB Shutdown if more than one match of VPN.
In 64-bit Kernel mode, the *xkuseg* access is controlled by UX bit & the *xkseg* access is controlled by the SX bit. In 64-bit supervisor mode, *xsuseg* space access is controlled by UX bit. This means, the Address Space Access control and TLB miss exception vectors support separate page table for 32-bit and 64-bit programs	No such control for the 32-bit & 64-bit programs available
No CP0 hazards	Hazards be't CP0 instructions
CP0 Registers:	
LLAddr Register removed because it is not necessary	LLAddr Register available & necessary
Added Diagnostic register	Not available

Differences between R10000 and R4400

R10000	R4400
Added Frame Mask Register to masking of write into TLB[PFN]	Framemask not available
Added Performance Counter Registers	Performance info from State Output pins.
Context/XContext do not share PTE Base	Context/XContext shares PTE Base
WatchHi adjusted to accommodate 40 bits of physical address.	WatchHi smaller.
EntryLo/Hi bigger with new cache d coherency attributes	EntryLo/Hi smaller
CacheErr & ECC are different	
Config Register is different	
Status Register is different	
Cache Management	*Cache Management*
CACHE Instructions has no hazards cause they are serialized	Hazards between CACHE/CP0 instructions
No support for:	Support for -
Create Dirty Exclusive	Create Dirty Exclusive
Fill I	Fill I
Hit Writeback	Hit Write back
Hit Virtual	Hit Virtual
Additional Instructions:	
Index Load/Store Data (no support needed for CE bit)	No Index Ld/St Data Need CE bit
Read/Write is 36-bits pre-decoded instructions to PICache	No pre-decode
Cache Barrier instruction added	Not applicable
Might bring lines in the cache	

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Differences between R10000 and R4400

R10000	R4400
that never get used	No speculation; so always gets used.
System Interface	***System Interface***
Four outstanding Processor Req.	Single request except if "Cluster Request" selected
Cluster bus configuration with eight outstanding request.	
Request can depend on the speculation and might not be used.	
Request can come in different order in different conditions; but never indeterminate for the any condition.	Request always in order
No link address retained bit	Link retained bit needed
SysIntf & SCIntf de-coupled by Input Buffers	No input buffers so speed on SysIntf dependent on SCIntf.
Data ordering subblock	Data ordering programmable
Eliminate Request	No Eliminate Request
Open Drain option on System Intf.	No open drain
Uncached Attributes added	No Uncache Attribute
No output buffer slew rate adjustment.	Output buffer slew rate adjustment possible
"Globally Performed" pin added	No "Globally Performed" pin
SCache Interface	***SCache Interface***
Same hardware for 16Wd & 32Wd block size	Need to worry about the LSB of the Tag.
SSRAM, HSTL interface	SRAM CMOS/TTL interface
No uncompelled slave state	Uncompelled releases of the bus

Differences between R10000 and R4400

R10000	R4400
Exceptions	***Exception***
Aliasing prevented by the hardware so no Virtual Coherency Exception	Aliasing handled by Virtual Coherency Exception
Can identify between the Soft Reset & NMI	Cannot differentiate be't Soft Reset and NMI
Initialization	***Initialization***
Mode bits entered in parallel	Mode bits entered serially
Must write into the logical registers before reading	Not necessary to initialize register files
Interrupts	***Interrupts***
Five hardwares by ext. request using single cycle.	Six hardware interrupts via write req. or pins
No hardware interrupts pins	NMI via write or pin
No NMI by write (only pins)	Timer Interrupt muxed by an external write
Timer Interrupt not muxed by external write	No Performance Counters (State bits at the output)
Performance counter causes Timer Interrupt	
Error protection	***Error protection***
If DE bit is set, cache hits are taken when error is detected; so cache can get corrupted. Units detects & corrects but exceptions are not taken. No real need to set DE bit.	If DE bit is set - always takes cache miss if uncorrectable error is detected.
Option for parity check on SCache read on the first pass.	Data ECC - 8-bits for each DWd
Data ECC - 9-bits for QWd	Single format Cache Error Reg.

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Differences between R10000 and R4400

R10000	R4400
Separate Cache Error Reg. format for each caches & system intf.	
System Interface has ECC only.	System Interface has a choice of ECC or Parity.
UncorrErr*/CorrErr* signals.	
Clocks	***Clocks***
Input clock SysClk is used to clock external logic	RClock & TClock available to clock external logic.
SClkTap to adjust SCClk.	
Not applicable	SyncIn/SyncOut to adjust T/RClock
MISC	***MISC***
External Intf. CMOS/TTL or HSTL	External Intf. CMOS/TTL
Can bring lines in the cache that may never be used	Lines in cache will always be used