mips
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# Power Management in R4300i

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## 1.1 Introduction

The availability of high-performance RISC microprocessors at low costs is allowing these devices to be used in a variety of consumer applications. These range from 3D video games to hand held personal computers, also referred to as PDAs. In addition to high-performance, consumer applications also demand low system power consumption. As a key component in consumer systems operating anywhere from 50MHz to 100MHz, the microprocessor needs to be designed to minimize both static and dynamic power consumption. This paper describes the design features in the MIPS R4300i which allows the microprocessor to operate with very low power consumption.

## 1.2 Power Management in the R4300i

The R4300i is designed with the objective of achieving low power dissipation. Several architecural features achieve this objective. In addition, there are other features that allow overall system power dissipation to be reduced as well.

The architectural features that make the R4300i suitable in consumer and battery-operated systems are

- Write-Back cache policy
- Segemented instruction and data caches
- Instruction cache buffer
- Single execution unit for integer and floating point operations
- Reduced pipeline stages

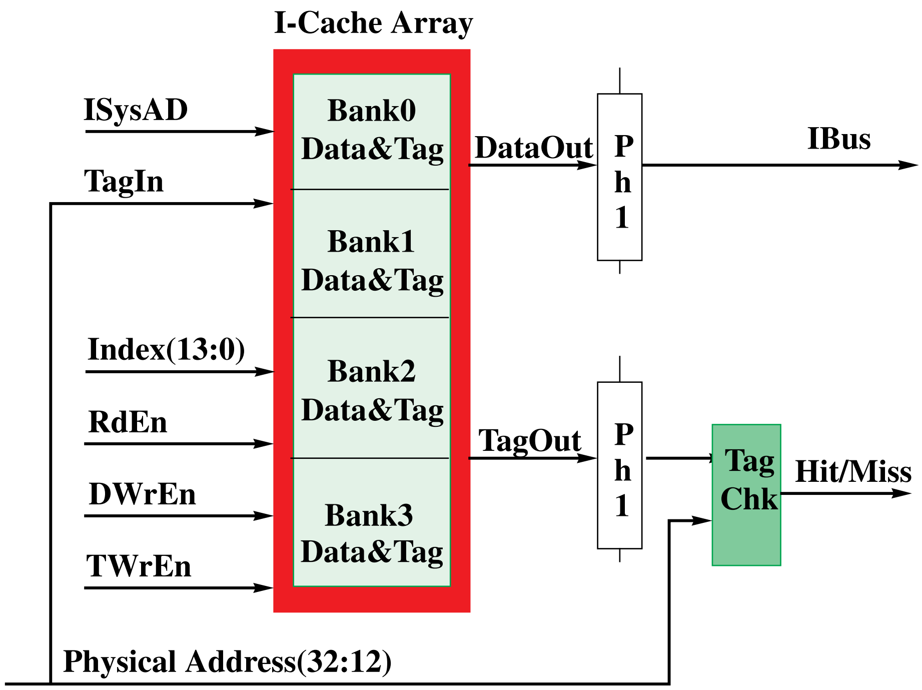
### 1.2.1 Write-Back Cache Policy

In a write-back cache policy, block writes are written only to the block in cache. The data in cache is written to main memory only if the information in the cache line is replaced with a read or write operation to a different address. This is different from the write-through policy where every write to the cache is also written to main memory. Therefore, the frequency of write operations on the system bus is much higher. Since every write operation is not written to main memory at the same time, the write-back scheme uses less memory bandwidth. This reduces power consumption on the bus as the number of times the system bus switches is reduced.

### 1.2.2 Segmented Instruction and Data Caches

The R4300i has a 16KB instruction cache (I-cache) and an 8KB Data cache (D-cache). Both caches are direct mapped. The I-cache is organized as four banks of 4KB each and the D-cache is organized as four banks of 2KB each. The banks are selected by the high order index address bits. Each bank is 64-bits wide. Only the bank that contains the requested address is turned “on” during a cache access. Figure shows the organization of the I-cache. The D-cache is similarly organized as two banks of 4KB each.

Figure 1 I-cache Block Diagram




### 1.2.3 I-cache buffer

The I-cache is accessible in one pipeline cycle. Each access fetches a 64-bit word. As the instruction is only 32-bits wide, each access to the I-cache in effect, fetches two instructions. I-cache accesses occur every other cycle during sequential cache accesses as the next instruction has already been fetched and stored in a buffer. This reduces the frequency of accesses to the I-cache. The exceptions to this are when there is a jump or a branch instruction.

### 1.2.4 Integrated Execution Unit

The execution unit in the R4300i contains all the hardware resources necessary to execute all of the MIPS integer and floating point instructions. This not only reduces the size of the chip but also reduces the interconnect capacitance. The execution unit also uses a modular design approach to further reduce dynamic power consumption. Control logic is partitioned into small independent block; each responsible for a set of instructions. When relevant instructions are not in the instruction stream, the corresponding control blocks are inactive. Also, when functional elements in the data path are idle, they operate on a constant selected to minimize power dissipation, instead of on data from the bus.

## 1.3 System Design Considerations To Reduce Power Consumption

The system designer can further reduce power consumption by using several features in the R4300i. The R4300i supports both normal and reduced power operation modes. Transitions from one of these modes to the other is caused by the software setting or resetting of the RP bit in the coprocessor zero (CP0) status register (shown in Figure 2). When the RP bit is set to a 1, the pipeline clock frequency and the system interface clock frequency gets reduced by a factor of 4. After a cold reset, the RP bit is set to a 0.

Figure 2 CP0 Status Register

Status Register = register 12 of CP0


RP -> Reduced Power. Changes clock quarter speed
0 = Normal operation; 1 = reduced speed operation

To operate in a reduced power mode, the software must flush all the cache locations using the cache operations provided by the MIPS instruction set. The R4300i also allows easy access to all the registers including general purpose registers, floating point registers, and CP0 registers. These states must also be saved and restored accordingly.

Setting the RP bit to 1 reduces the clock frequency of SClock and TClock by a factor of four. The clocks (PClock, SClock, and TClock) will switch frequency within one to sixteen MasterClock cycles after the software has performed a move operation to the status register in CP0. If an external controller has any timing dependent features (such as DRAM refresh), the controller must provide a mechanism so that software can accommodate the frequency change.

## 1.4 Power Dissipation

The R4300i is designed to operate with a supply voltage of 3.3V. The R4300i normally dissipates around 1.8Watts at a frequency of 100MHz. Under reduced power mode, the power dissipation is reduced by about 25% of normal operating mode. At 100MHz operating frequency, this translates to about 1.2Watts.

## 1.5 Summary

The low power dissipation of the 64-bit R4300i along with the architectural features that enable high performance makes it an ideal candidate for demanding consumer applications. The R4300i uses both internal logic and circuit design techniques to reduce power overall and also provides the system designer with the flexibility to further reduce power dissipations.