FE3000A

AT CPU CONTROL LOGIC

- 100% hardware and software compatible to the IBM PC-AT
- Wait State Generator-Internal or External
- 8284 and 82284-compatible Clock Generator
- 256K and 1MB RAM support
- Look-ahead Memory Commands
- Compatible with Intel 80286 processor
- 82288-compatible Bus Controller
- Supports 6, 8, and 10MHz clock speeds
- Refresh or DMA controls
- HCMOS technology
- Error Detector Controls

Introduction

The Faraday FE3000A AT CPU controller integrated circuit provides designers with the capability to build an AT-compatible single-board computer. The chip reduces cost through lower power requirements, increased reliability, and reduced board size. The FE3000A replaces 53 IC components with a single CMOS 84-pin J-leaded package. The FE3000A is used in conjunction with the Faraday FE3010, the AT peripheral controller, the FE3020 AT address buffer, and the FE3030 AT data buffer.

Figure 1 illustrates a block diagram of the FE3000A AT CPU controller integrated circuit. Refer to Table 1 for the pin descriptions shown in Figure 2.

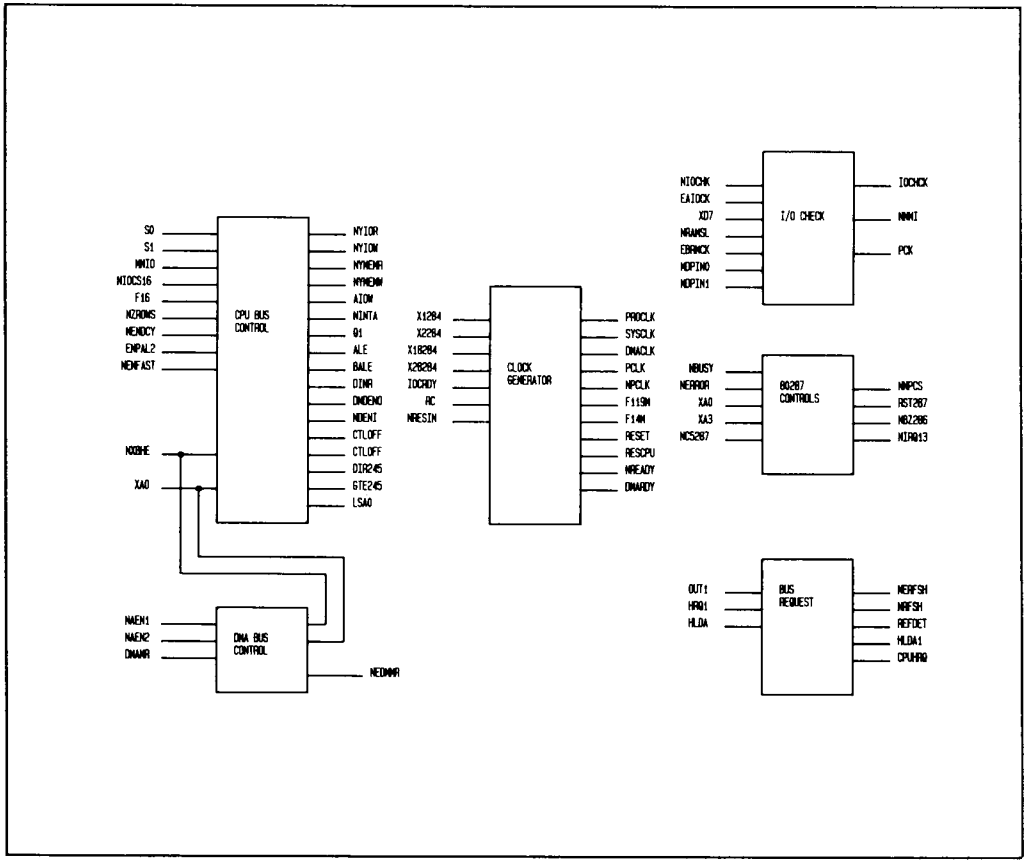

Figure 1. FE3000A Block Diagram

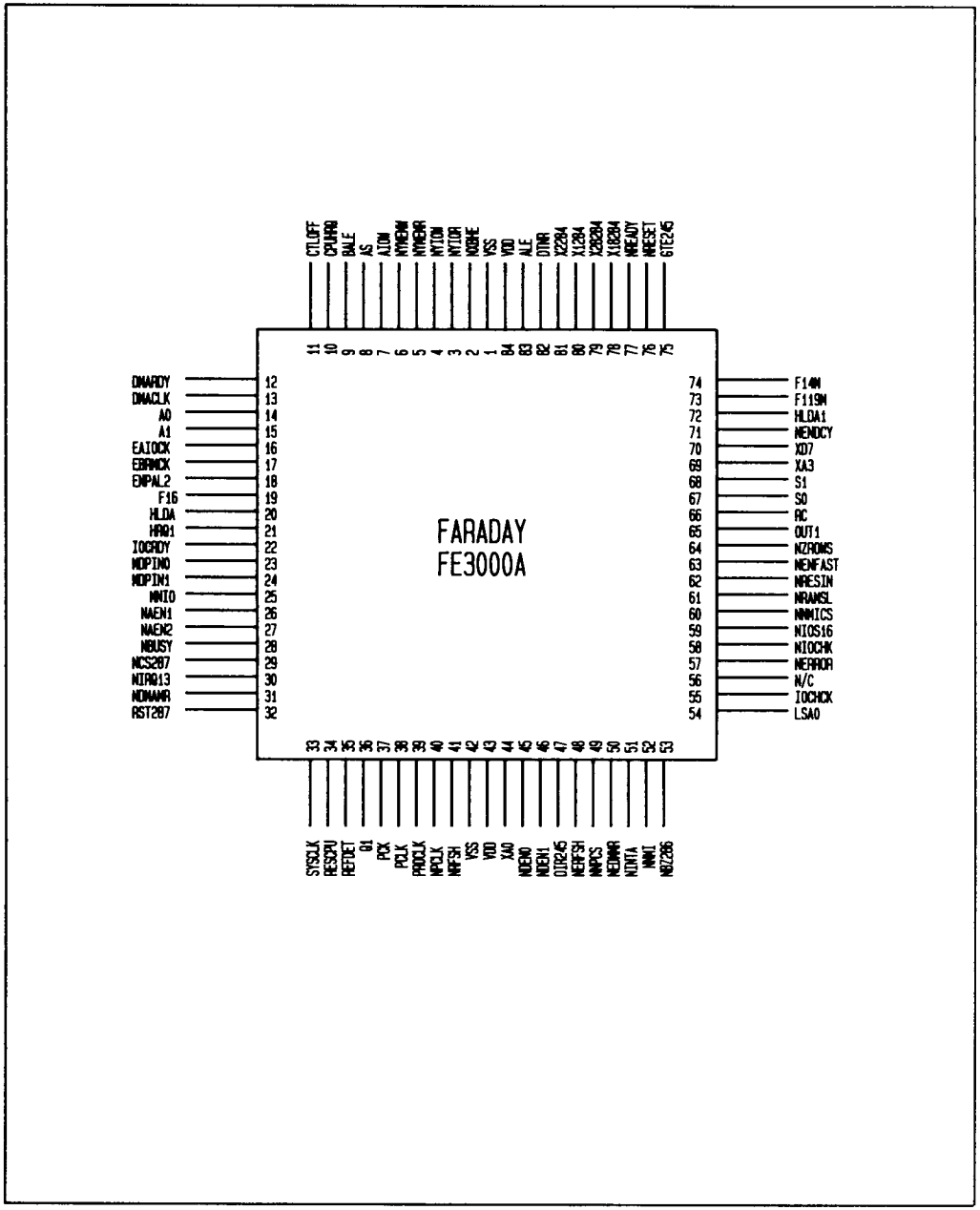

Figure 2. FE3000A Pin Diagram

Table 1. Pin Description

Pin	Type	Symbol	Function
1		V_{SS}	GROUND
2	I/O	NXBHE	BUS HIGH ENABLE Active low Indicates the current bus cycle will transfer a byte on the upper byte.
3	I/O	NYIOR	I/O READ COMMAND Active low Indicates a read of an I/O device.
4	I/O	NYIOW	I/O WRITE COMMAND Active low Indicates a write of an I/O device.
5	I/O	NYMEMR	MEMORY READ COMMAND Active low Indicates a read of memory.
6	I/O	NYMEMW	MEMORY WRITE COMMAND Active low Indicates a write of memory.
7	O	AIOW	EXTENDED I/O WRITE COMMAND Active high Used for external wait state generator.
8	O	AS	REAL TIME CLOCK ALE Active high Used to latch the address in the clock calendar chip (Motorola 146818).
9	O	BALE	BUS ADDRESS LATCH ENABLE Active high Or of ALE and HLDA.
10	O	CPUHRQ	BUS HOLD REQUEST TO 80286 Active high Bus request to 80286 CPU caused by refresh or a DMA cycle.
11	O	CTLOFF	DATA LATCH CONTROL Active high Latch data bits 0-7 of first bus cycle of a word transfer on a byte device.
12	O	DMARDY	READY TO DMA Active high Indicates that the DMA may complete its cycle.
13	O	DMACLK	CLOCK TO DMA DEVICES Clock in sync with and half the frequency of the SYSCLK. (i.e., 3, 4, or 5 MHz)
14	I	A0	80286 ADDRESS A0 Active high Address bit 0 from the 80286.

Table 1. Pin Description *(cont'd)*

Pin	Type	Symbol	Function
15	I	A1	80286 ADDRESS A1 Active high Address bit 1 from the 80286.
16	I	EAIOCK	ENABLE I/O CHECK Active high Enable error signal from the expansion bus.
17	I	EBRMCK	ENABLE RAM PARITY CHECK CONTROL Active high Enable parity check from on board RAM.
18	I	ENPAL2	DISABLE EXTERNAL WAIT STATE Active high Disables external wait state generator.
19	I	F16	16-BIT MEMORY OPERATION Active high Indicates that the current memory cycle is a 16-bit transfer.
20	I	HLDA	HOLD ACKNOWLEDGE FROM THE 80286 Active high Indicates that the 80286 has released the bus in response to a CPUHRQ signal.
21	I	HRQ1	HOLD REQUEST Active high Bus request from a DMA controller.
22	I	IOCRDY	EXPANSION BUS READY Active high Signal from the expansion bus to indicate that the current cycle may complete.
23	I	MDPIN0	PARITY BIT FROM RAM BANK 0 Parity bit from on board RAM bits 0-7.
24	I	MDPIN1	PARITY BIT FROM RAM BANK 1 Parity bit from on board RAM bits 8-15.
25	I	MNIO	MEMORY I/O SELECT Active high Signal from the 80286 indicating the next cycle is a memory cycle.
26	I	NAEN1	ENABLE DMA CHANNELS 0-3 TO USE DATA BUS Active low
27	I	NAEN2	ENABLE DMA CHANNELS 5-7 TO USE DATA BUS Active low
28	I	NBUSY	BUSY STATUS ASSERTED BY 80287 Active low
29	I	NCS287	80287 I/O CHIP DECODE Active low
30	O	NIRQ13	INTERRUPT REQUEST 13 Active low Co-processor error.

Table 1. Pin Description *(cont'd)*

Pin	Type	Symbol	Function
31	I	NDMAMR	DMA MEMORY READ COMMAND Active low Memory read command from a DMA controller.
32	O	RST287	RESET TO 80287 Active high
33	O	SYSCLK	SYSTEM CLOCK System clock in phase with and half the frequency of the PROCLK (i.e.; 6, 8, or 10MHz).
34	O	RESCPU	RESET TO 80286 Active high Reset to CPU from a command to exit protected mode or an external reset.
35	O	REFDET	REFRESH DETECT Signal that toggles each time there is a refresh cycle to the RAM.
36	O	Q1	START OF BUS CYCLE Active high Indicates start of a bus cycle to the external wait state generator.
37	O	PCK	PARITY CHECK Active high Indicates a RAM parity error has been detected.
38	O	PCLK	CLOCK TO 8042
39	O	PROCLK	PROCESSOR CLOCK TO 80286 Clock twice the processor speed. (i.e., 12, 16, or 20MHz).
40	O	NPCLK	INVERTED CLOCK TO 8042
41	I/O	NRFSH	REFRESH CYCLE Active low Indicates the current bus cycle is a RAM refresh cycle.
42		VSS	GROUND
43		VDD	+5 VOLTS SUPPLY
44	I/O	XA0	ADDRESS A0 Active high System address bit 0.
45	O	NDEN0	GATE DATA 0-7 Active low
46	O	NDEN1	GATE DATA 8-15 Active low
47	O	DIR245	BYTE SWAP DIRECTION Signal to control byte swap direction on a 16-bit transfer on an 8-bit device.

Table 1. Pin Description *(cont'd)*

Pin	Type	Symbol	Function
48	O	NERFSH	ENABLE REFRESH ADDRESS Active low Signal to enable the refresh address to the address bus during a RAM refresh cycle.
49	O	NNPCS	80287 CHIP SELECT Active low
50	O	NEDMMR	ENABLE DMA MEMORY READ Active low Gates a memory read to the bus during a DMA cycle.
51	O	NINTA	INTERRUPT ACKNOWLEDGE Active low Interrupt acknowledge to the interrupt controllers.
52	O	NNMI	NMI OUTPUT TO 80286 Active low Non-maskable interrupt to 80286.
53	O	NBZ286	80287 BUSY TO 80286 Active low
54	O	LSA0	LATCHED SYSTEM ADDRESS A0 Active high System address bit 0 during a CPU bus cycle.
55	O	IOCHCK	I/O DEVICE ERROR Active high Indicates an error from the expansion bus.
56	N/C		UNUSED Must be left open.
57	I	NERROR	80287 ERROR Active low Error from the 80287.
58	I	NIOCHK	I/O CHECK Active low Error signal from the expansion bus.
59	I	NIOS16	16-BIT I/O TRANSFER Active low Signal from the expansion bus to indicate that the current bus cycle is a 16-bit I/O transfer.
60	I	NNMICS	NMI PORT DECODE Active low Decode of NMI enable port.
61	I	NRAMSL	ON BOARD RAM DECODE Active low
62	I	NRESIN	RESET IN Active low External reset is used to generate a system reset.

Table 1. Pin Description *(cont'd)*

Pin	Type	Symbol	Function
63	I	NENFAST	ENABLE LOOK AHEAD DECODE Active low Causes early generation of memory read and write signals with zero wait states.
64	I	NZROWS	ZERO WAIT STATES Active low Indicates the current bus cycle should have no wait states.
65	I	OUT1	TERMINAL COUNT OF TIMER CHANNEL 1 Active high Terminal count from timer channel 1.
66	I	RC	RESET TO CPU 80286 Active high Input to generate RESET to CPU.
67	I	S0	BUS CYCLE STATUS S0 FROM 80286
68	I	S1	BUS CYCLE STATUS S1 FROM 80286
69	I	XA3	ADDRESS A3 Active high System address bit 3.
70	I	XD7	SYSTEM DATA BUS BIT 7 Active high
71	I	NENDCY	TERMINATE CURRENT CYCLE Active low Signal from external wait state generator to end the current bus cycle.
72	O	HLDA1	HOLD ACKNOWLEDGE TO DMA Active high Hold acknowledge to one of DMA controllers.
73	O	F119M	1.19 MHz CLOCK TO TIMER
74	O	F14M	14.318 MHz SIGNAL TO EXPANSION BUS
75	O	GTE245	ENABLE BUS SWAP Active low Gates data during the swap of a byte on a 16-bit transfer on an 8-bit device.
76	O	NRESET	RESET TO SYSTEM LOGIC Active low
77	O	NREADY	SYNCHRONIZED READY TO CPU Active low Ready to CPU indicating that the current bus cycle may terminate.
78	I	X18284	CRYSTAL TO 8284 CLOCK GENERATOR
79	O	X28284	CRYSTAL TO 8284 CLOCK GENERATOR
80	I	X1284	CRYSTAL TO 82284 CLOCK GENERATOR
81	O	X2284	CRYSTAL TO 82284 CLOCK GENERATOR

Table 1. Pin Description *(cont'd)*

Pin	Type	Symbol	Function
82	O	DTNR	DATA DIRECTION CONTROL Active low A low indicates a bus read cycle.
83	O	ALE	ADDRESS LATCH ENABLE Active high Signal to latch the address from the 80286.
84		V_{DD}	+5 VOLTS SUPPLY

FUNCTIONAL DESCRIPTION

Error Detection

This block looks for parity errors from on-board memory or errors from the PC Bus and generates a non-maskable interrupt (NMI). The NMI may be enabled by writing a 0 to port 070H with data bit 7. It can be disabled by writing a 1 to port 070H with data bit 7. It is disabled by a system reset.

On-board parity is checked by sending the two parity bits from the RAM parity generator to MDPIN0 and MPDIN1. The EBRMCK and NRAMSL signals are used to enable the parity checking.

The IOCK signal indicates an error from the bus. It is gated by the EAIOCK signal.

80287 Controls

This block contains I/O decodes for the 80287 coprocessor, and handles the BUSY and ERROR signals from the 80287 coprocessor. If an error is detected, an interrupt can be generated by using the NIRQ13 signal.

Bus Request

This block contains circuitry to arbitrate between a DMA request and a refresh request.

When a refresh or DMA request is made, a CPUHLRQ signal will be sent to the 80286 and an HLDA will be received in reply.

For a DMA request (IHRQ1), an HLDA1 will be generated to the DMA controller.

For a refresh requedst (OUT1), an NERFSH will be generated to enable the refresh address to the bus. AN NYMEMR signal will then be generated to cause a memory refresh cycle.

Clock Generator

This block contains two clock generators. One generates clocks for the CPU, DMA, and 8042 keyboard conroller. This clock generator can run at 6, 8, or 10 MHz. The DMA clock is half the CPU clock; that is, 3, 4, or 5 MHz.

The other clock generator provides a 14.31818 MHz clock for the PC bus and the 8254 timer contained in the FE3010 AT peripheral controller. This clock contains circuitry to synchronize the CPU reset, the CPU ready, the DMA ready, and the system reset.

This block also contains a wait state for compatibility with the PC and AT Bus. You can disable the internal wait state generator by means of a jumper (ENPAL2). You can add an external wait state generator by using the Q1 signal to start a wait state generator and sending an NENDCY to the FE3000A to end the cycle. Refer to the Crystal Circuit Diagram shown in Figure 3.

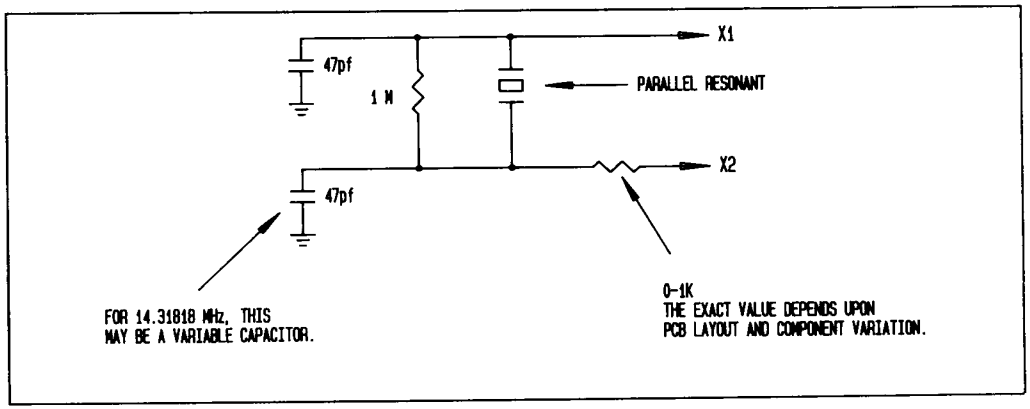

Figure 3. FE3000A Crystal Circuit Diagram

CPU Bus Control

This block generates the bus controls for CPU, DMA, and refresh cycles. This includes data buffer controls, address latch controls, BHE and address 0 generation, I/O read and write signals, and memory read and write signals. Refer to Figure 4, Write Bus Cycle, and Figure 5 Read Bus Cycle.

Controls are provided for data bits 0-7 (CTLOFF, NDEN0, DTR), data bits 8-15 (NEDN1, DTR), and the byte swap buffer (CTLOFF, DIR245).

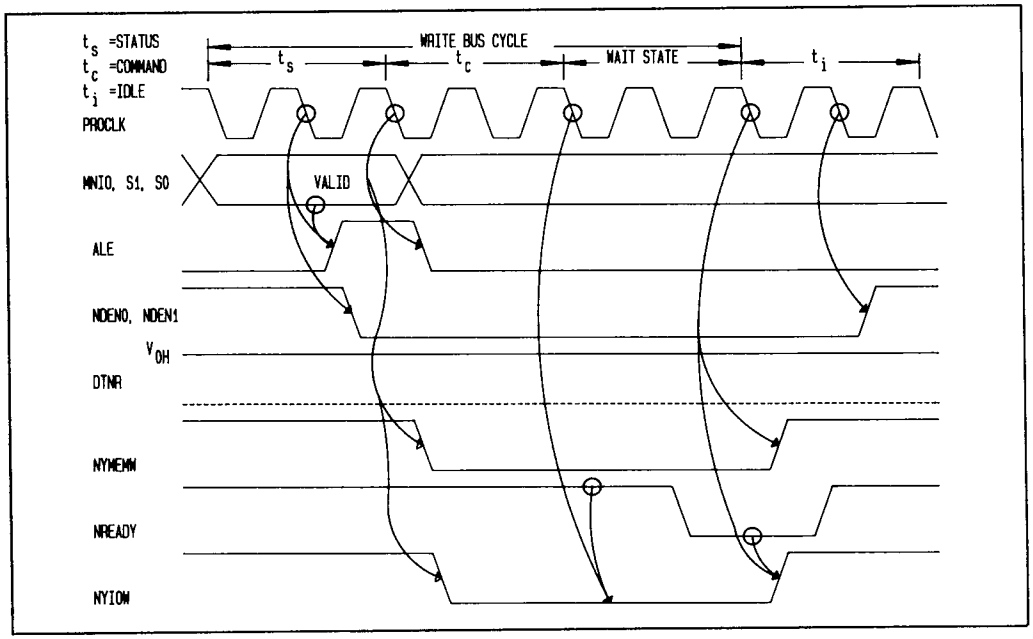

Figure 4. FE3000A Write Bus Cycle

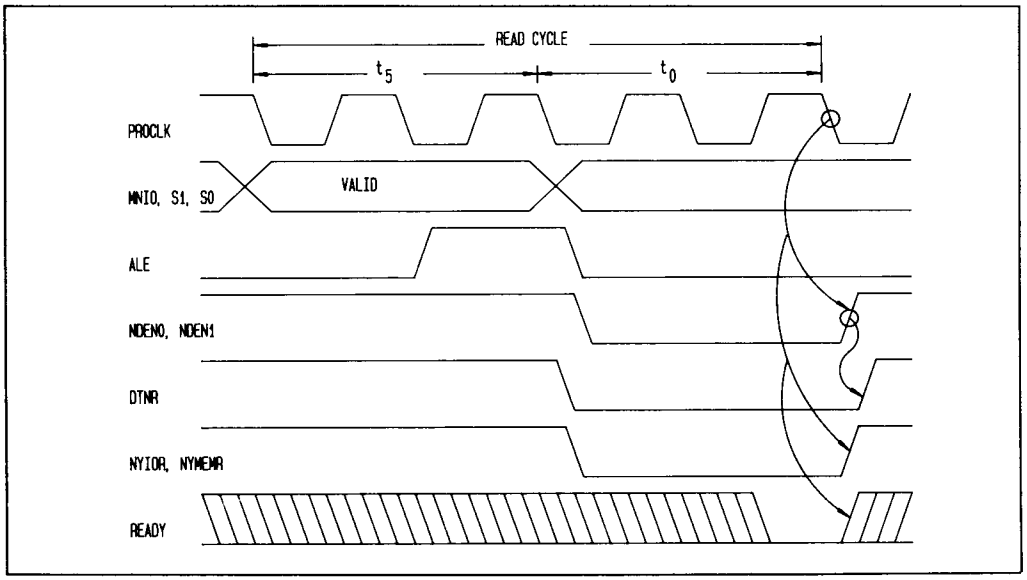

Figure 5. FE3000A Read Bus Cycle

Table 2. Bus Cycles

MNIO	S1	S0	Type of Bus Cycle
0	0	0	Interrupt acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	None; not a status cycle
1	0	0	Halt or shutdown
1	0	1	Memory read
1	1	0	Memory write

Table 3. Absolute Maximum Ratings*

T_A = +25 ° C

Power supply voltage, V_{DD}	3.0 V to +7.0 V
Power dissipation, PDMAX @V_{DD}=5.25V	200mW
Current, IDD @V_{DD}=5.25V	38mA
Input voltage, VI	0.0V to V_{DD} + 0.3V
Output voltage, VO	0.0 V to V_{DD} + 0.3V
Operating temperature, TOPT	0 ° C to +70 ° C
Storage temperature, TSTG	-40 ° C to +125 ° C

*Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Capacitance

T_a = +25 ° C, V_{DD} = 0V

		Limits			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Condition**
Input capacitance	CI		10	pF	fc = 1 MHz unmeasured pins returned to 0V
I/O capacitance	CIO		15	pF	

Table 5. DC Characteristics

T_A = 0 ° C to +70 ° C, V_{DD} = +5V ± 5%

DC Characteristics
[A0,A1,EAIOCK,EBRMCK, ENPAL2, F16, HLDA, HRQ1, IOCRDY, MDPIN0,MDPIN1, MNI0, NAEN1, NAEN2, NBUSY, NCS287, NDMAMR,NENDCY,NENFAST,NERROR,NIOCHK, NIOS16, NNMICS, NRAMSL, NZROWS, OUT1, RC, S0, S1, XA3, XD7]

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	V_{IL}	V_{SS}	0.8	V	V_{DD} = 5V ± 5%
Input high voltage	V_{IH}	2.0	V_{DD}	V	V_{DD} = 5V ± 5%
Input low current	I_{IL}	-35.0	-200.0	V	V_{IN} = 0.0V
Input high current	I_{IH}		40.0	uA	V_{IN} = V_{DD}

DC Characteristics
[NXBHE, NYIOR, NYIOW, NYMEMR, NYMEMW, XA0]

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	V_{IL}	V_{SS}	0.8	V	V_{DD} = 5V ± 5%
Input high voltage	V_{IH}	2.0	V_{DD}	V	V_{DD} = 5V ± 5%
Input low current	I_{IL}		-10.0	uA	VIN = 0.0V
Input high current	I_{IH}		10.0	uA	VIN = V_{DD}
Output high voltage	V_{OH}	2.4		V	I_{OH} = -4.0mA
Output low voltage	V_{OL}		0.4	V	I_{OL} = 4.0mA
Output impedance	IOZ	-10.0	10.0	uA	0V < V_{OUT} < V_{DD}
Short circuit current low state	IOSL	25	120	MA	VO = V_{DD}
Short circuit current high state	IOSH	-15	-85	MA	VO = V_{SS}

Table 5. DC Characteristics *(cont'd)*

T_A = 0 ° C to +70 ° C, V_{DD} = +5V ± 5%

DC Characteristics
[X1284, X1884]

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	V_{IL}	V_{SS}	0.3*V_{DD}	V	V_{DD} = 5V ± 5%
Input high voltage	V_{IH}	0.7*V_{DD}	V_{DD}	V	V_{DD} = 5V ± 5%
Input low current	I_{IL}		-10.0	uA	V_{IN} = 0.0V
Input high current	I_{IH}		10.0	uA	V_{IN} = V_{DD}

DC Characteristics
[NRESIN]

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	V_{IL}	V_{SS}	1.0	V	V_{DD} = 5V ± 5%
Input high voltage	V_{IH}	4.0	V_{DD}	V	V_{DD} = 5V ± 5%

Table 5. DC Characteristics *(cont'd)*

$T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 5\%$

DC Characteristics

[NRFSH]

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	V_{IL}	V_{SS}	1.0	V	$V_{DD} = 5V \pm 5\%$
Input high voltage	V_{IH}	4.0	V_{DD}	V	$V_{DD} = 5V \pm 5\%$
Input low current	I_{IL}		-10.0	uA	$V_{IN} = 0.0V$
Input high current	I_{IH}		10.0	uA	$V_{IN} = V_{DD}$
Output high voltage	V_{OH}	2.4		V	$I_{OH} = -8.0mA$
Output low voltage	V_{OL}		0.4	V	$I_{OL} = 8.0mA$
Output current	IOZ	-10.0	10.0	uA	$0V < V_{OUT} < V_{DD}$

DC Characteristics

[AS, BALE, CPUHRQ, CTLOFF, DMACLK, DMARDY, F119M, F14M, HLDA1, IOCHCK, LSA0, NBZ286, NEDMMR, NINTA, NNMI, PCK, REFDET, RESCPU, RST287, SYSCLK, NIR013, Q1, GTE245, DIR245]

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	V_{OL}		0.4	V	$I_{OL} = 2.0mA$
Output high voltage	V_{OH}	2.4		V	$I_{OH} = -2.0mA$

DC Characteristics

[X2284, X28284]

Parameter	Symbol	Min	Max	Unit	Test Condition
Output high voltage	V_{OH}	2.4		V	$I_{OH} = -8.0mA$
Output low voltage	V_{OL}		0.4	V	$I_{OL} = 8.0mA$

Table 5. DC Characteristics *(cont'd)*

T_A = 0 ° C to +70 ° C, V_{DD} = +5V ± 5%

DC Characteristics
[AIOW,ALE,DTNR,NDEN0,NDEN1,NERFSH,NNPCS,NPCLK, NREADY, NRESET, PCLK, PROCLK, Q1]

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	V_{OL}		0.4	V	I_{OL} = 4.0mA
Output high voltage	V_{OH}	2.4		V	I_{OH} = -4.0mA

Table 6. AC Characteristics

TA = 0 ° C to +70 ° C, V_{DD} = +5V ± 5%, Output load capacitance=85pF Processor clock at 8MHz.

Symbol	Parameter	Min	Max	Unit
t0	PROCLK PERIOD (P)	62.5	62.5	ns
t1	PROCLK low period.	½p-0.3	½p-1	ns
t2	PROCLK high period.	½p+0.3	½p+1	ns
t3	PCLK high delay from PROCLK falling edge.	1	5	ns
t4	PCLK low delay from PROCLK falling edge.	2	9	ns
t5	NPCLK low delay from PCLK rising edge.	2	10	ns
t6	NPCLK high delay from PCLK falling edge.	-1	-2	ns
t7	MNI0, S1, S0 set-up time.	4	24	ns
t8	ALE active high delay from PROCLK falling edge.	2	10	ns
t9	ALE inactive low delay from PROCLK falling edge.	3	12	ns
t10	NDEN0, NDEN1 (WRITE) active low delay from PROCLK falling edge.	6	31	ns
t11	NDEN0, NDEN1 (WRITE) inactive high delay from PROCLK falling edge.	4	19	ns
t12	NYMEMW active low delay from PROCLK falling edge.	4(3)	20(12)	ns
t13	NYMEMW inactive high delay from PROCLK falling edge.	4	17	ns
t14	NREADY active low delay from PROCLK falling edge.	5	22	ns
t15	NREADY inactive high delay from PROCLK falling edge.	4	18	ns
t16	NYIOW active low delay from PROCLK falling edge.	4	18	ns
t17	NYIOW inactive high delay from PROCLK falling edge.	3	14	ns
t18	NDEN0, NDEN1 (READ) inactive low delay from DTNR falling edge.	3	14	ns

Table 6. AC Characteristics *(cont'd)*

TA = 0 ° C to +70 ° C, V_{DD} = +5V ± 5%, Output load capacitance=85pF Processor clock at 8MHz.

Symbol	Parameter	Min	Max	Unit
t19	NDEN0, NDEN1 (READ) inactive high delay from PROCLK falling edge.	3	14	ns
t20	DTNR active low delay from PROCLK falling edge.	3	17	ns
t21	DTNR inactive high delay for NDEN0, NDEN1 rising edge.	3	15	ns
t22	NYIOR active low delay from PROCLK falling edge.	4	17	ns
t23	NYIOR inactive high delay from PROCLK falling edge.	3	14	ns
t24	NYMEMR active low delay from PROCLK falling edge. See *Note*.	5(3)	21(13)	ns
t25	NYMEMR inactive high delay from PROCLK falling edge.	4	18	ns
t26	NINTA active low delay from PROCLK falling edge.	7	33	ns
t27	NINTA inactive high delay from PROCLK falling edge.	4	20	ns
t28	NINTA inactive high delay from CTLOFF rising edge.	2	6	ns
t29	NINTA active low delay from CTLOFF falling edge.	0	-1	ns
t30	NYIOR inactive high delay from CTLOFF rising edge.	2	6	ns
t31	NYIOR active low delay from CTLOFF falling edge.	0	-1	ns
t32	NYIOW inactive high delay from CTLOFF rising edge.	3	11	ns
t33	NYIOW active low delay from CTLOFF falling edge.	1	3	ns
t34	NYMEMR inactive high delay from CTLOFF rising edge.	2	10	ns
t35	NYMEMR active low delay from CTLOFF falling edge.	0	2	ns
t36	RST287 (RESET) active high delay from PROCLK falling edge.	4	19	ns

Table 6. AC Characteristics *(cont'd)*

TA = 0 ° C to +70 ° C, V_{DD} = +5V ± 5%, Output load capacitance=85pF Processor clock at 8MHz.

Symbol	Parameter	Min	Max	Unit
t37	RST (NYIOW) active high delay from PROCLK falling edge.		-5	ns
t38	NBZ286 (RESET) inactive high delay from PROCLK falling edge.	6	29	ns
t39	NBZ286 (NYIOW) inactive high delay from PROCLK falling edge.		0	ns
t40	RESCPU active high delay from PROCLK falling edge.	3	15(24)	ns
t41	RESCPU inactive low delay from PROCLK falling edge.	6	34	ns
t42	RESCPU active high delay from PROCLK falling edge in Shutdown.	5	24	ns
t43	RESCPU active high delay from PROCLK falling edge in Reset.	7	37	ns

Note: 1 NYMEMR and NYMEMW in look-ahead Decode mode.

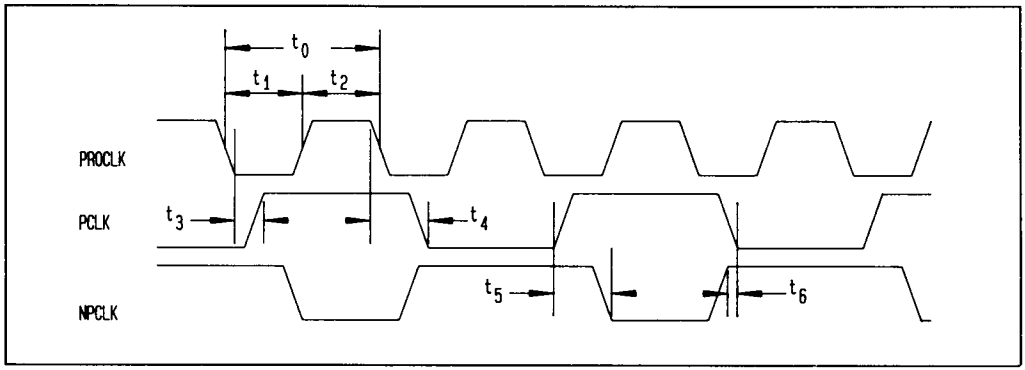

Figure 6. FE3000A Clock Timing Diagram

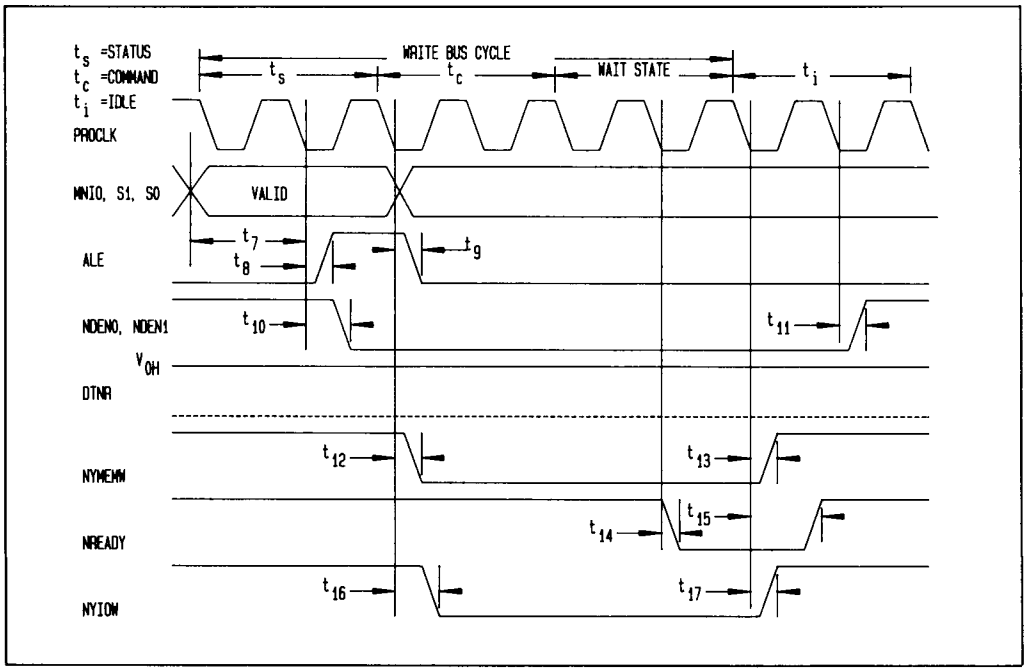

Figure 7. FE3000A Write Bus Cycle

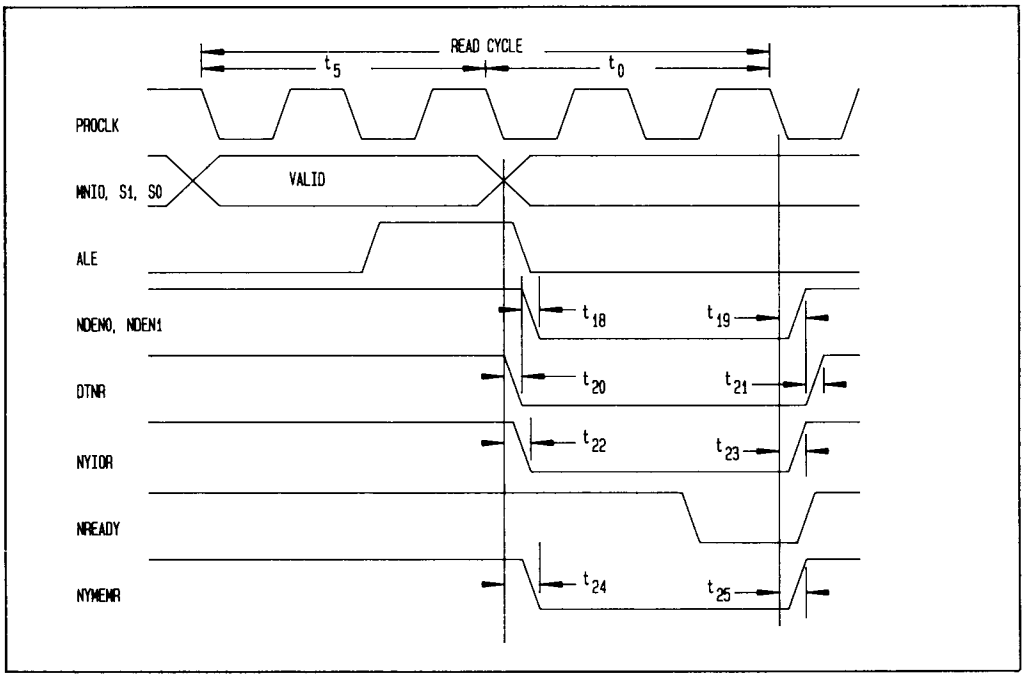

Figure 8. FE3000A Read Cycle

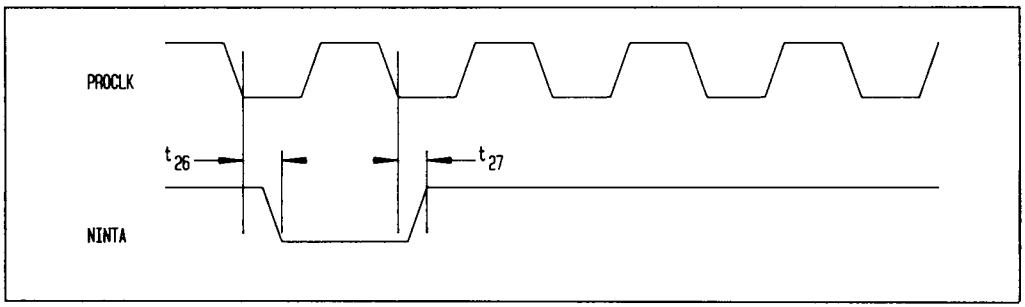

Figure 9. FE3000A NINTA1 Diagram

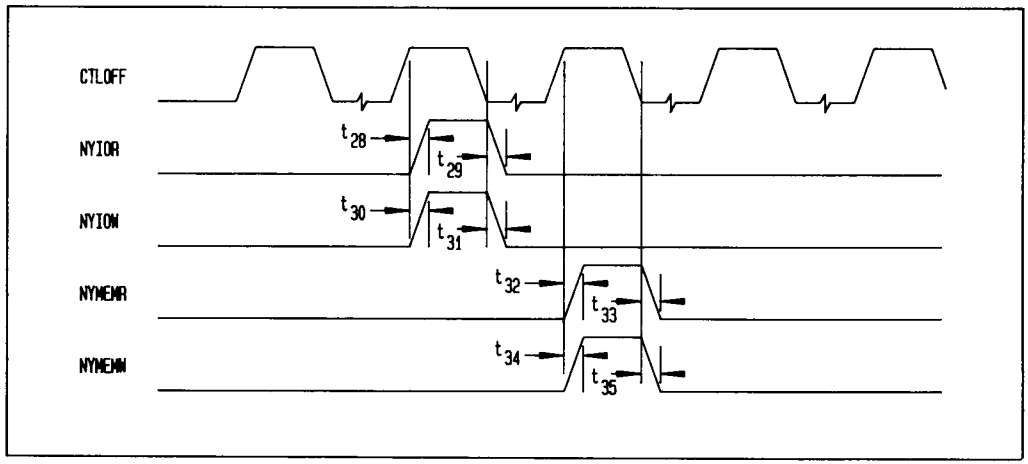

Figure 10. FE3000A Control Diagram

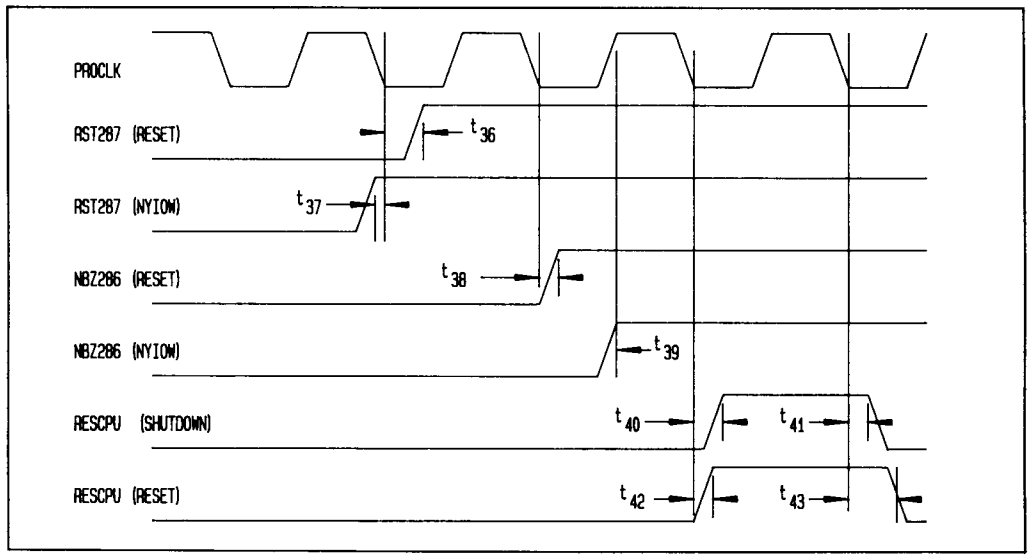

Figure 11. FE3000A Reset Diagram

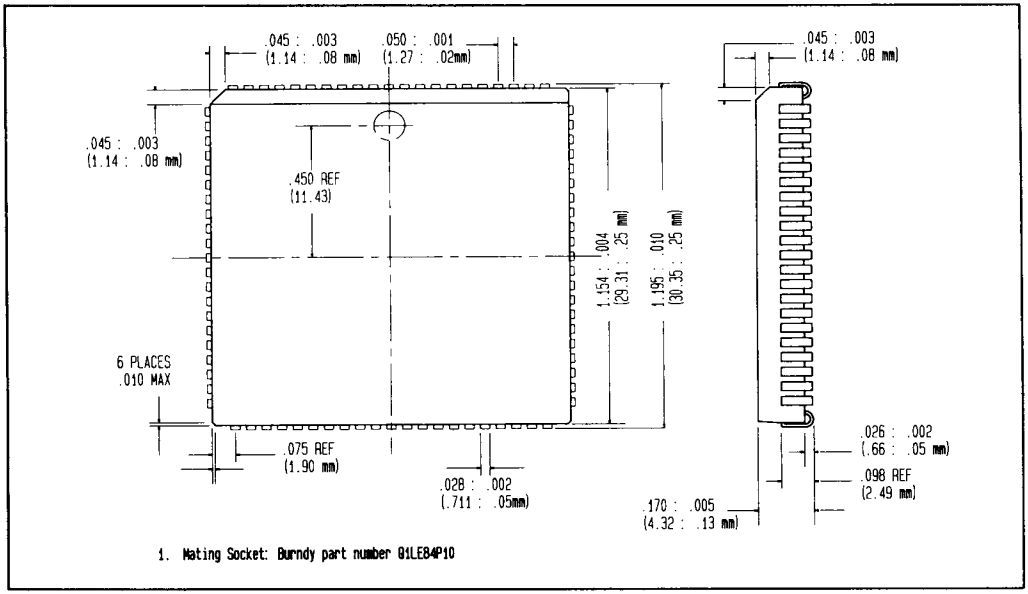

Figure 12. FE3000A 84-Pin Plastic Chip Carrier (J-bend Leads)

Copyrights

Intel[R] is a registered tradename of Intel Corporation.

Faraday Electronics, Inc. reserves the right to make changes or improvements to the equipment, software, hardware, and documentation described herein at any time and without notice.

Disclaimer Notice

Faraday Electronics, Inc. makes no warranty of any kind with regard to this material. Faraday Electronics, Inc. assumes no responsibilities for any errors that may appear in this document. Faraday Electronics, Inc. makes no commitment to update or keep current the information contained in this document. Contact the factory for information regarding the status of this product.

CORPORATE HEADQUARTERS
Faraday Electronics, Inc.
749 North Mary Avenue
Sunnyvale, CA 94086
408-749-1900 Telex 706738
FAX #408-738-1671

EUROPEAN HEADQUARTERS
Faraday Electronics Ltd.
Technology House
Easthampstead Road, Bracknell
Berkshire, RG12 1LX, England
Telephone 0344 486677
Telex 847096 EMDAL
FAX #44 344 485210

WD1473F 8/87 5M

P/N 01012700 A